76200-402

MODELS T200 AND T300
TRIDENT DISK DRIVES
THEORY OF OPERATION

January 1981

Century Data Systems

TECHNICAL MANUAL CHANGE/ERRATA SHEET

MANUAL TITLE		
T200/T300 THEORY OF OPERATION		
PART NUMBER: 76200-402	DATE: 2/4/81	CHANGE NO.: 1
SHEETS: 1 of 1	AUTHORIZATION:	

This Errata Sheet, Change 1, authorizes the following changes to the subject manual:

- Page 2-6, paragraphs one through three; change 160 microsecnds to 200 microseconds.
- Page 2-6, Figure 2-6; change one-shot time from 160 us to 200 us, and change art file number in lower right hand corner from 11805A to 11805B.

RECORD OF REVISIONS	
REVISION	NOTES
0	ORIGINAL ISSUE
1	INCORPORATES MISCELLANEOUS CORRECTIONS
2	INCORPORATES MISCELLANEOUS ADDITIONS AND CORRECTIONS

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the technical manuals, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION 1
INTRODUCTION

This manual contains functional and detail theory descriptions for the Trident Model T200 and Model T300 Disk Drives. These disk drives handle removable disk packs that have 19 recording surfaces and provide nominal data storage capacity of 200 megabytes (T200) or 300 megabytes (T300).

The theory discussions in this manual are primarily intended for training Trident maintenance technicians and for reference purposes. However, they may also be of value to other technical or applications personnel who require a basic knowledge of Trident Disk Drive theory.

RELATED DOCUMENTS

Century Data Systems provides the following related documents to support the T200/T300 Disk Drives:

Installation and Operation	76200-2XX
Maintenance	76200-3XX
Parts Catalog	76200-5XX
Performance Specifications	76200-9XX
Maintenance Diagrams	76200-7XX
Model T2000B Exerciser	76203-1XX

MANUAL ORGANIZATION

The contents of this manual are divided into seven sections:

- Section 1 — Introduction
- Section 2 — Power Sequencing
- Section 3 — Input Interface and Control
- Section 4 — Head-Positioning Servo System
- Section 5 — Read/Write System
- Section 6 — Status and Error Detection
- Section 7 — Power System

Section 1 describes the Trident Disk Drive in general, basic model differences, and principles of operation — in other words, a general overview of these devices and how they work.

The other sections contain detail theory of operation for each functional system of the disk drives, noting optional differences where applicable. Event sequence timing diagrams, block diagrams, and simplified logic diagrams using MIL-STD-806 type logic symbols support the text in these sections. Signal names are sometimes followed by a slash (/) mark; this mark indicates a low-active signal. This level of logic theory is intended to fill the needs of the maintenance technician for trouble diagnosis and fault isolation.

EQUIPMENT DESCRIPTION

Model T200 and Model T300 Disk Drives are a part of the Trident family of modular memory devices used for mass storage in data processing systems, particularly minicomputer class systems. Both models use the same removable, 19-surface disk packs as the storage medium, although packs in use are not interchangeable between the two disk drives due to differences in bit packing densities.

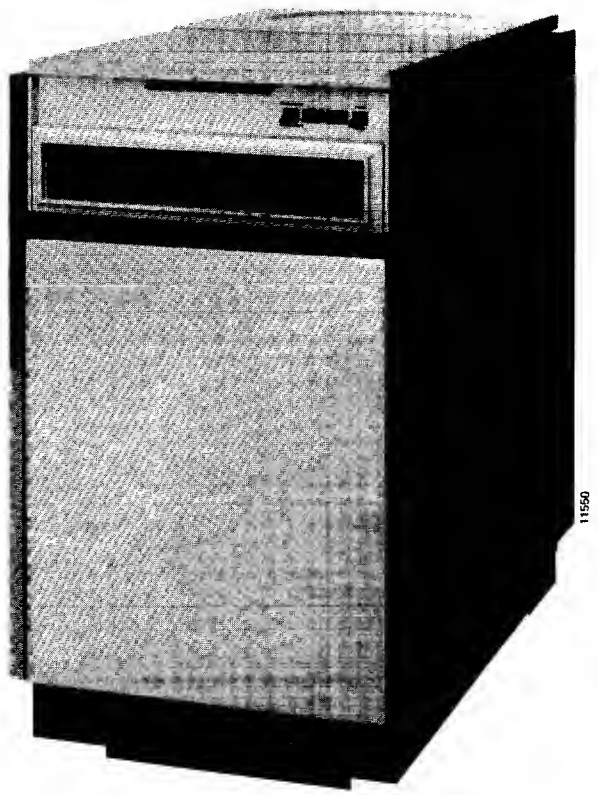

Figure 1-1. Trident T200/T300 Disk Drive

The Trident Model T200 and Model T300 are built around the same equipment chassis with the majority of electrical and mechanical parts common to both. As a matter of fact, the Model T200 can be upgraded in the field to a Model T300 with a conversion kit available from the manufacturer. Both present a standard electrical interface and are interchangeable in every way except for data transfer rates and storage capacities. Table 1-1 lists the equipment specifications for both models.

TABLE 1-1. EQUIPMENT SPECIFICATIONS

Disk Pack	CDS P/N 16988-201 (T200) CDS P/N 16988-301 (T300)
Disk Pack Capacity	208.1 megabytes (T200); Unformatted 312.1 megabytes (T300);
Recording Format	Fixed or variable length
• Recording Method	Triple frequency, bit serial
• Interface Data Transfer	NRZ bit serial
• Data Transfer Rate	806 kilobytes/sec (6.45 megabits/sec) for T200; 1209 kilobytes/sec (9.68 megabits/sec) for T300
• Data Bit Cell Time	155 nanoseconds (T200) 103.3 nanoseconds (T300)
Rotational Speed	3600 rpm ±3%
Rotational Latency	
• Average	8.33 milliseconds
• Maximum	17.2 milliseconds
Head Positioning Method	Servo-controlled linear motor
Recording Surfaces	19 data surfaces
Recording Cylinders	815
Cylinder Spacing	0.0027 inch (nominal)
Bit Density	4040 bits/inch (nominal) inner track (T200) 6060 bits/inch (nominal) inner track (T300)
Track Density	370 tracks/inch
Tracks Per Pack	15485
Access Time	
• Minimum	6.0 milliseconds/cylinder to cylinder
• Average	30 milliseconds/random number of seeks
• Maximum	55 milliseconds/815-cylinder seek
Start/Stop Time	
• Start	20 seconds (drive ready, nominal)
• Stop	30 seconds (nominal)

Model T300 Disk Drives have a 50 percent greater data storage capacity than Model T200 Disk Drives. The greater capacity is a result of higher bit packing density: 6060 bits per inch (bpi) for the Model T300 versus 4040 bpi for the Model T200. Because of the higher frequencies and lower levels of the recorded signals, thc circuits associated with the writing, reading, and data recovery, although similar in concept, are of different design.

FUNCTIONAL DESCRIPTION

Figure 1-2 is a general block diagram that is applicable to both these modesl of Trident Disk Drive and shows the functional systems that execute disk drive operations and the interfacing command, data, and status lines that connect the disk drive to the controller.

Electrical and electromechanical components of the Trident Disk Drive fall into six major systems by function. These six functional systems are as follows:

- Interface and Control System
- Disk Pack Drive System
- Head-Positioning Servo System
- Read/Write System
- Status and Error Detection System
- Power Supply System (not shown on block diagram)

The block diagram should be studied carefully before proceeding further, as it provides a good overview of disk drive organization and contains concise statements of the operations performed by each functional system. It should be noted that the control commands sent by the controller to the disk drive are received by the Interface and Control System and redirected to one or more of the other four systems for execution. However, a few operations, namely power-up and power-down sequencing, involve several systems and require direct communication between systems for sequence control. Also note that the Status and Error Detection System functions as a collection point for most status information returned to the controller.

It will be helpful to return to the block diagram from time to time during the remainder of the discussion in Section 1 and associate each operation with the flow of control signals between systems.

PRINCIPLES OF OPERATION

Certain hardware and operational characteristics of the disk drive must be understood as a basis for more detailed study of functional systems and circuit design. The following principles of operation provide this necessary background information.

Disk Pack and Head Configuration

The disk pack consists of twelve 14-inch disks that are firmly attached to a central hub. Only the 10 inner disks serve recording functions; the top and bottom disks protect the recording surfaces. Nineteen of the inner disk surfaces are used for reading and writing; the remaining surface is a prerecorded read-only, track-reference servo surface. See Figure 1-3. The disk pack is a precision instrument manufactured to close tolerances and is carefully balanced to ensure a stable recording surface.

Nineteen recording heads and the servo (read only) head are rigidly mounted to the positioning carriage, one

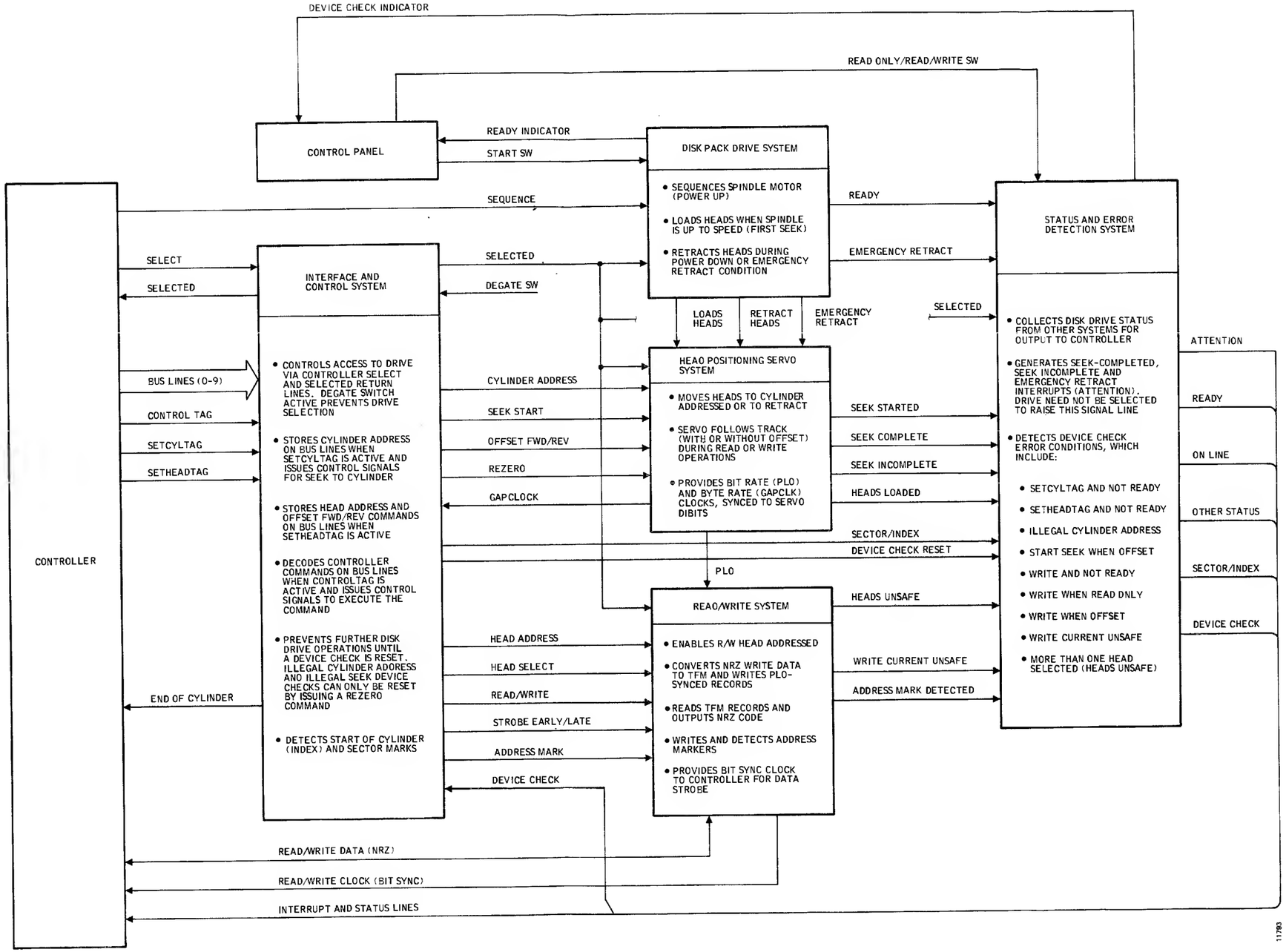

Figure 1-2. Disk Drive Systems Block Diagram

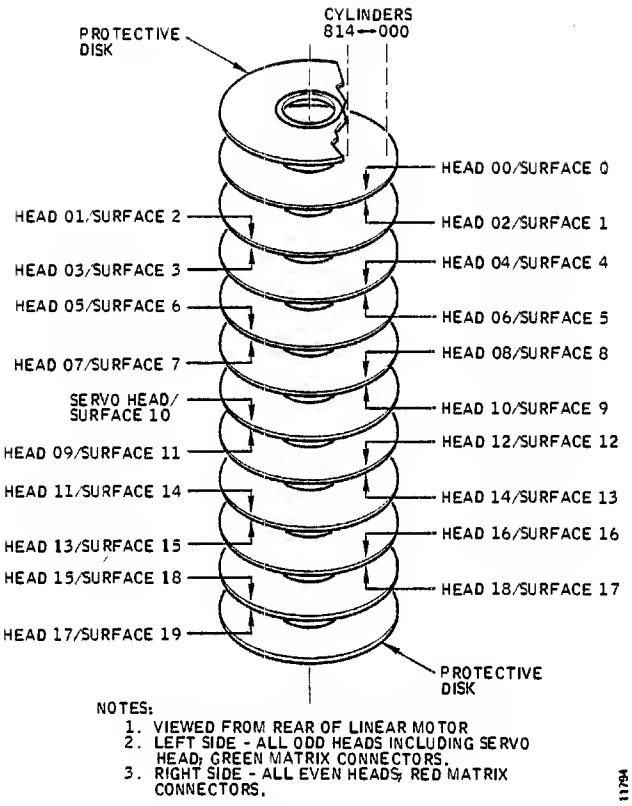

Figure 1-3. Disk Pack and Head Configuration

above the other. Spacing between the disks allows the comb-like arrangement of read/write heads to move into and out of the pack. Recording heads are aligned so that their recording pole pieces can be positioned axially to within 50 microinches of the servo head pole piece at a selected point (cylinder 496) on the pack surface.

As the disk spins, a high-pressure airflow is generated at the disk surface. The heads are spring loaded to counteract this force from the disk surface so that the balance between the two forces allows the head to *fly* on the boundary layer thus created. During normal operation, the heads never contact the disk surface and, therefore, no wear occurs. The boundary air layer moves up and down with minute irregularities in the disk surface and the head floats with these changes so that the spacing of the head-to-disk surface remains constant at approximately 30 microinches.

Servo and Data Track Characteristics

The prerecorded servo surface is read continuously by the servo head whenever the heads are loaded onto the disk pack. Signals read by the servo head are processed by the disk drive to provide references for a variety of functions.

- Delineating guard band and recording zones on the disk recording surfaces
- Positioning and spacing data tracks on recording surfaces
- Providing track-crossing clocks for positive track location
- Providing on-track signal for track following (detent)
- Providing start-of-track index markers
- Providing a disk-speed-related, byte interval clock for precise data recording and recovery

Since the recording surface read/write heads are mechanically locked to the servo head through the carriage assembly, data tracks are positioned and spaced to a reference internal to each pack rather than externally to the disk drive. This technique minimizes pack-to-pack and drive-to-drive interchangeability problems.

The basic signal prerecorded on a servo track is one of alternate flux reversals spaced at 13,440 reversals per track (every 1.24 micorseconds, or 806 kHz, at speed). The only exception to this is the index marker that locates the start of each track. Index markers occur once per disk revolution and are detected from a 3-byte dead signal pattern recorded on each servo track of the disk pack.

See Figure 1-4. The flux reversal servo patterns of alternate odd and even servo tracks are displaced from one another by 180 degrees. Notice in the figure that the signals read when the servo head is over plus pattern tracks and minus pattern tracks exclusively are mirror images of one another and displaced by 180 degrees. The summation of these two signals, as would occur when the servo head is centered between tracks, is a distinctive symmetrical signal, called a dibit signal. This dibit signal is sampled and summed to produce a null voltage that serves as the on-track position reference. Figure 1-5 shows the spatial relationship between servo tracks and the data tracks produced by the read/write heads. Notice that the null (dibit) position of the servo head between tracks is the center line of the data tracks of that cylinder.

The servo surface format is shown in Figure 1-6. The outer periphery of the disk, where maximum boundary layer pressure occurs, is the head load zone where the heads first come into proximity to the disk surfaces and begin to fly. Moving inward, the servo head crosses an outer guard band that consists of 22 plus-pattern tracks. The significance of this guard band will be explained under the heading of the Head Load Operation.

The recording zone consists of 815 alternate minus and plus tracks. All these tracks (000 to 814) delineate cylinders that may be used for recording, but several are normally held as spares. And finally, there is an inner guard band that consists of 34 minus-pattern tracks.

Data track spacing is determined by servo track null points and is fixed at 0.0027 inch, center line-to-center

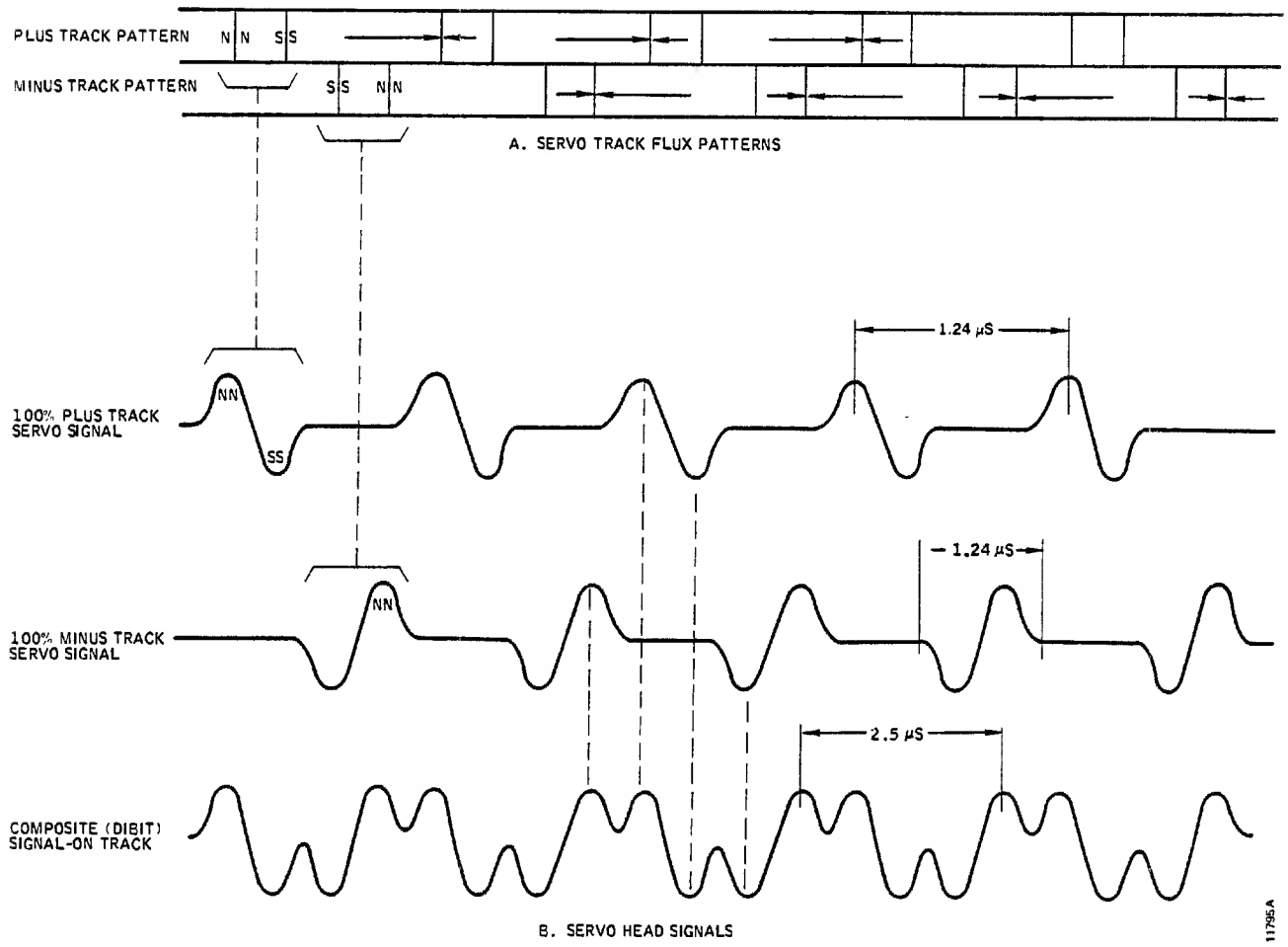

Figure 1-4. Servo Track Patterns and Dibit Signal

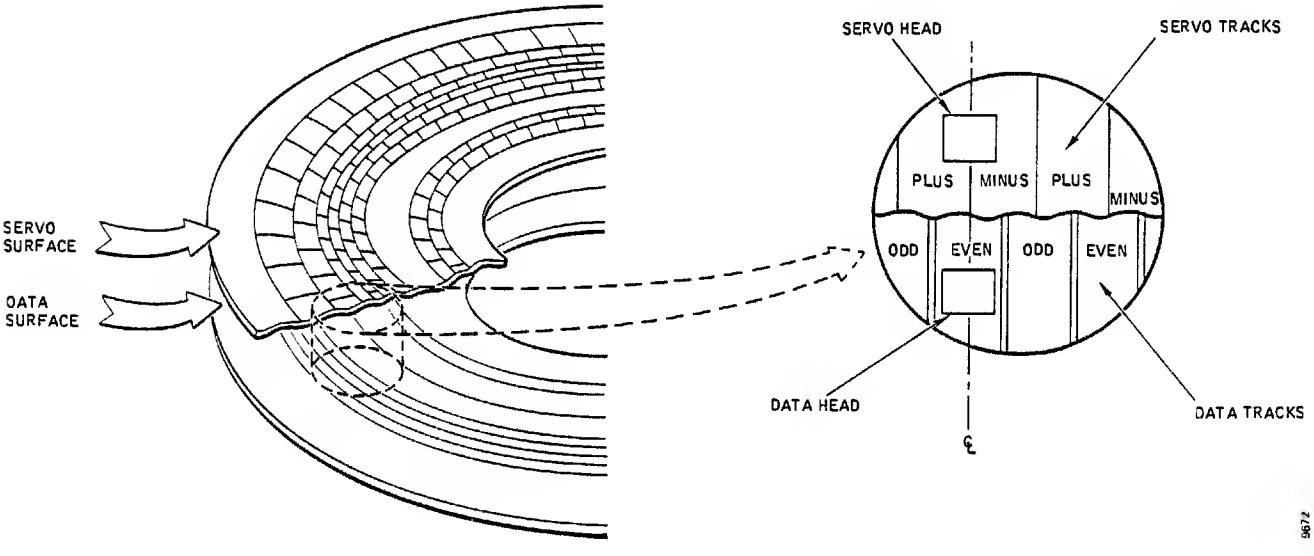

Figure 1-5. Servo and Data Track Alignment

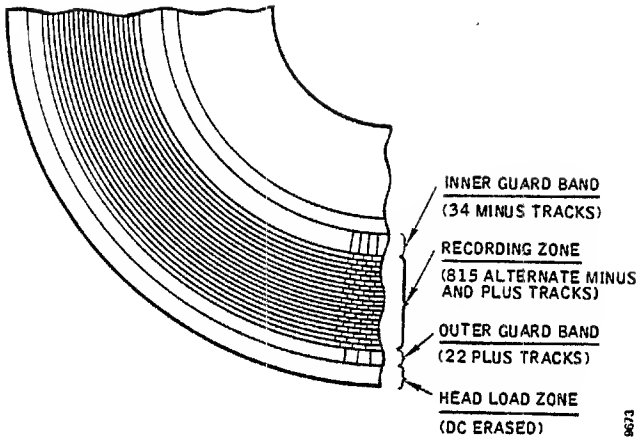

Figure 1-6. Servo Surface Format

line. Data track width is determined by read/write head width, head to surface distance, and flux strength (a function of write current). Nominally, track width is held to 0.0023 inch, leaving an intratrack gap of 0.0004 inch to minimize track crosstalk. Track density at these dimensions is 370 tracks per inch.

Head Load Operation

Initially, the linear motor bobbin and attached head carriage are in the fully retracted position with the heads drawn apart by camming surfaces on the head arms making contact with the cam tower. When power is turned on, the head load operation (also called first seek) is initiated automatically. The spindle motor begins to turn the disk pack counterclockwise.

As the spindle motor speed increases, an optical switch picks up pulses from a pattern of notches machined into the periphery of the brake disk. When the rate of these pulses indicates that the spindle is up to 80 percent of full speed, head loading is enabled. An exception is made when the spindle reaches speed in an inordinately short period of time (within 4 seconds), which would indicate that no disk pack was mounted on the spindle. In this case, head loading is inhibited, and power to the spindle motor is removed.

The linear motor bobbin, carriage, and heads begin moving forward at load speed (approximately 2 inches per second). When they reach the outer margin of the disk head load zone, the camming surfaces of the head arms leave the camming tower and allow facing heads to lower onto the disk surface boundary layer.

Track following becomes operational when the heads reach the outer guard band. Since all 22 tracks of this band are of the plus-track pattern, a positioning error signal is generated, which causes the linear motor to continue driving the heads in the inward (forward) direction. This will be discussed in greater detail under Track-Following Operation.

When the servo head approaches the track 000 position (intersection of the outer guard board and the minus-pattern track of the first recording zone track) the position error signal locks the servo head on cylinder 000. This completes the head load operation, and the disk drive goes into the ready condition, sending an Attention signal to the controller. The operation from power turn-on, to ready condition takes approximately 20 seconds.

Seek-to-Cylinder Operation

A cylinder is defined as all 19 recording tracks accessible to the read/write heads for a given track position of the servo head. Access to a given cylinder requires a new cylinder address to be transmitted and the start of seek operation to be commanded. Both these functions are under program control.

The controller initiates a programmed seek by placing an absolute cylinder address on the bus lines. It is compared with the current location cylinder address by an arithmetic subtractor to obtain a difference count. A minimum of 200 nanoseconds later, the controller raises the Set Cylinder Tag line (the delay is necessary to allow bus line and subtractor output settling). If the cylinder address on the bus lines is a legal address (not greater than 814), raising the tag line strobes the output of the subtractor into a difference counter. If the cylinder address is illegal, a device check will result. The new cylinder address is stored by the drive in its cylinder address register 350 nanoseconds after the Set Cylinder Tag line goes active.

The number strobed into the difference counter determines the number of tracks to be crossed to the new location and can be positive, negative, or zero. This number indicates magnitude only, not direction. If positive, forward (inward) seeking will be enabled. If negative, reverse (outward) seeking will be enabled. And if the difference count is zero, no seek operation will be enabled and an attention signal will be sent to the control unit.

Seek start is initiated by the controller when it drops the Set Cylinder Tag line a minimum of 800 nanoseconds later. If the difference count is not zero, dropping the tag line places the servo-positioning system into the seek-enable mode by changing from track following to velocity mode. Dropping the tag line also puts the drive in the not-ready condition.

The commanded velocity at which the forward or reverse seek operation starts is directly proportional to the magnitude of the difference count. Theoretically, a difference of 128 cylinders or more will cause the positioning servo system to be driven up to a maximum velocity (approximately 70 inches per second) from the start. In practice, this is not true because the acceleration phase of the operation requires more time than the deceleration phase. See Figure 1-7. Maximum velocity is controlled by feedback from a velocity transducer (tach rod and coil) in the linear motor.

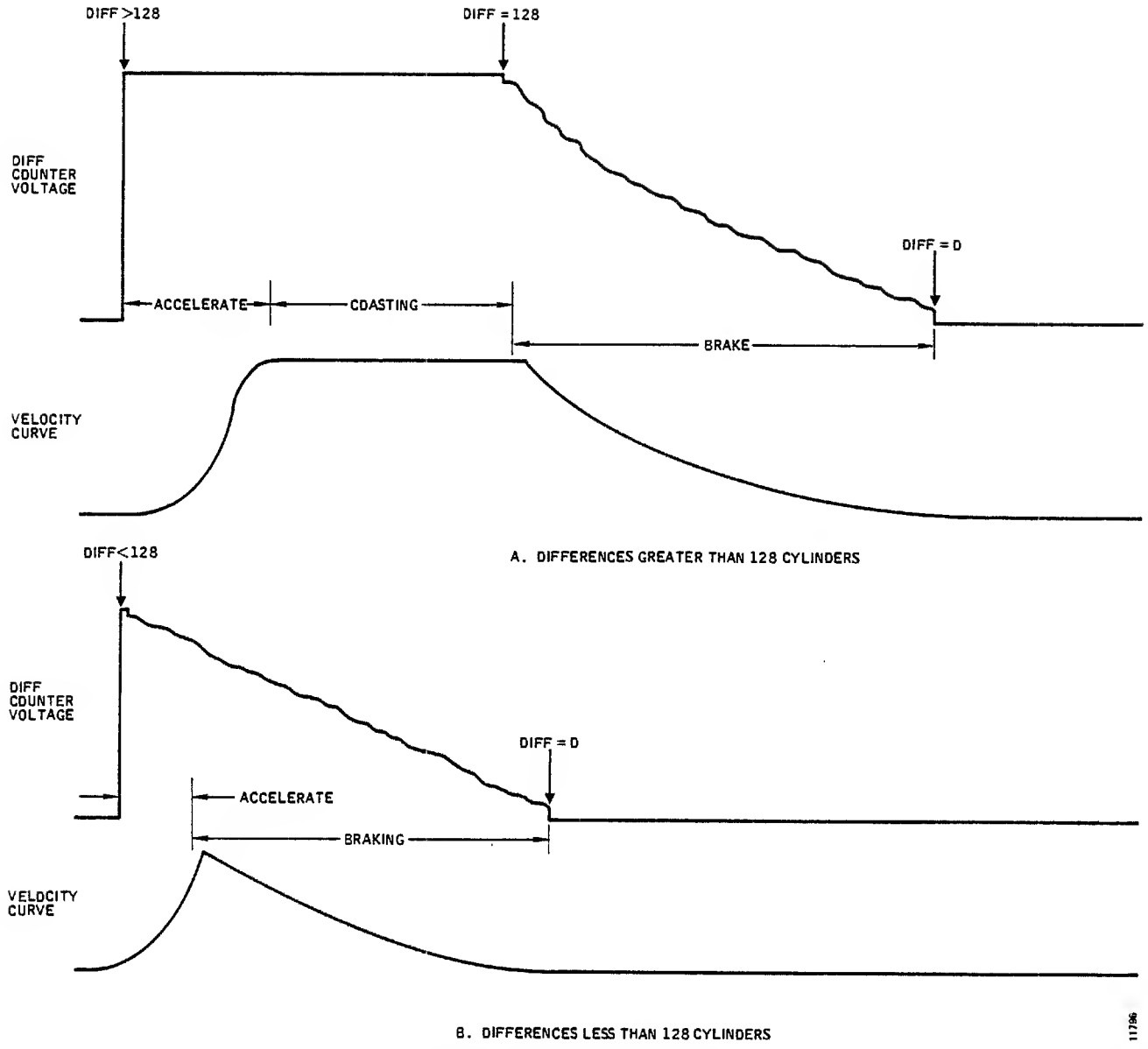

Figure 1-7. Seek Velocity Profiles

The digital difference count is converted by a digital-to-analog converter (DAC) to an analog voltage that is applied to a power switcher transistor network. When the applied analog voltage is greater than the feedback voltage from the velocity transducer, the power transistors switch in a +50-volt positive (forward) or a −50-volt negative (reverse) voltage to drive the motor. As the feedback voltage rises above the DAC output, the transistors switch in a voltage of opposite polarity to control the velocity of the head carriage. See Figure 1-8. The actual motor drive signal is, therefore, a series of pulses that are characterized by an ever-decreasing width as the head carriage nears the selected cylinder.

Each time the servo head crosses a servo track, a clock pulse is generated that reduces the difference count by one. Maximum commanded velocity will be maintained

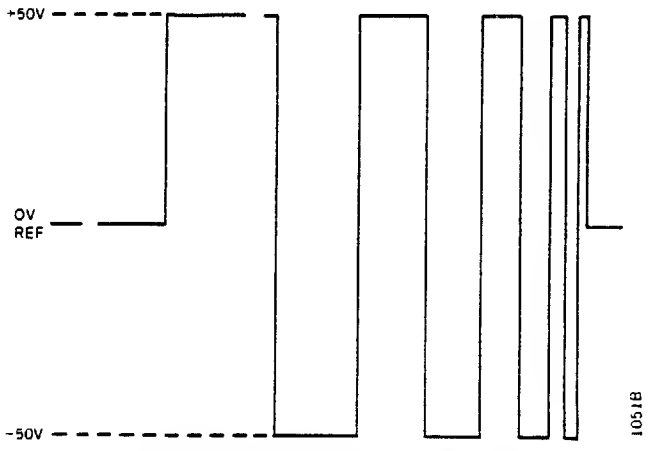

Figure 1-8. Motor Drive Signal

until the difference count is below 128. Below the count of 128, the drive signal to the servo system is reduced proportionally with the linear motor responding to balance out the signal with the output of the velocity transducer.

The tach feedback voltage, aided by the back EMF of the linear motor combine to slow the heads as they approach the correct cylinder (difference count of zero).

When the difference count is reduced to zero, the servo head will be within about 0.002 inch of the desired track, and the positioning system is switched back to the track-following mode. The servo system is then positioned exactly over the desired cylinder by the position error voltage derived from the dibit signal. Once this occurs, the seek-to-cylinder operation is complete, and following a 2.4-millisecond delay, the drive returns to the ready condition.

Positioning time for seeking to the next cylinder is normally 6 milliseconds, and for full seeks (814 cylinder difference) it is 55 milliseconds.

Track-Following Operation

Switching the positioning servo system to the track-following mode (detent on-track after first seek, programmed seek, or rezero) places the servo system under control of the dibit signal picked up by the servo head. As long as the dibit signal is symmetrical, indicating that the servo head is exactly centered between two adjacent recording zone servo tracks, the integrated position error voltage will be null, or zero volt. See Figure 1-9.

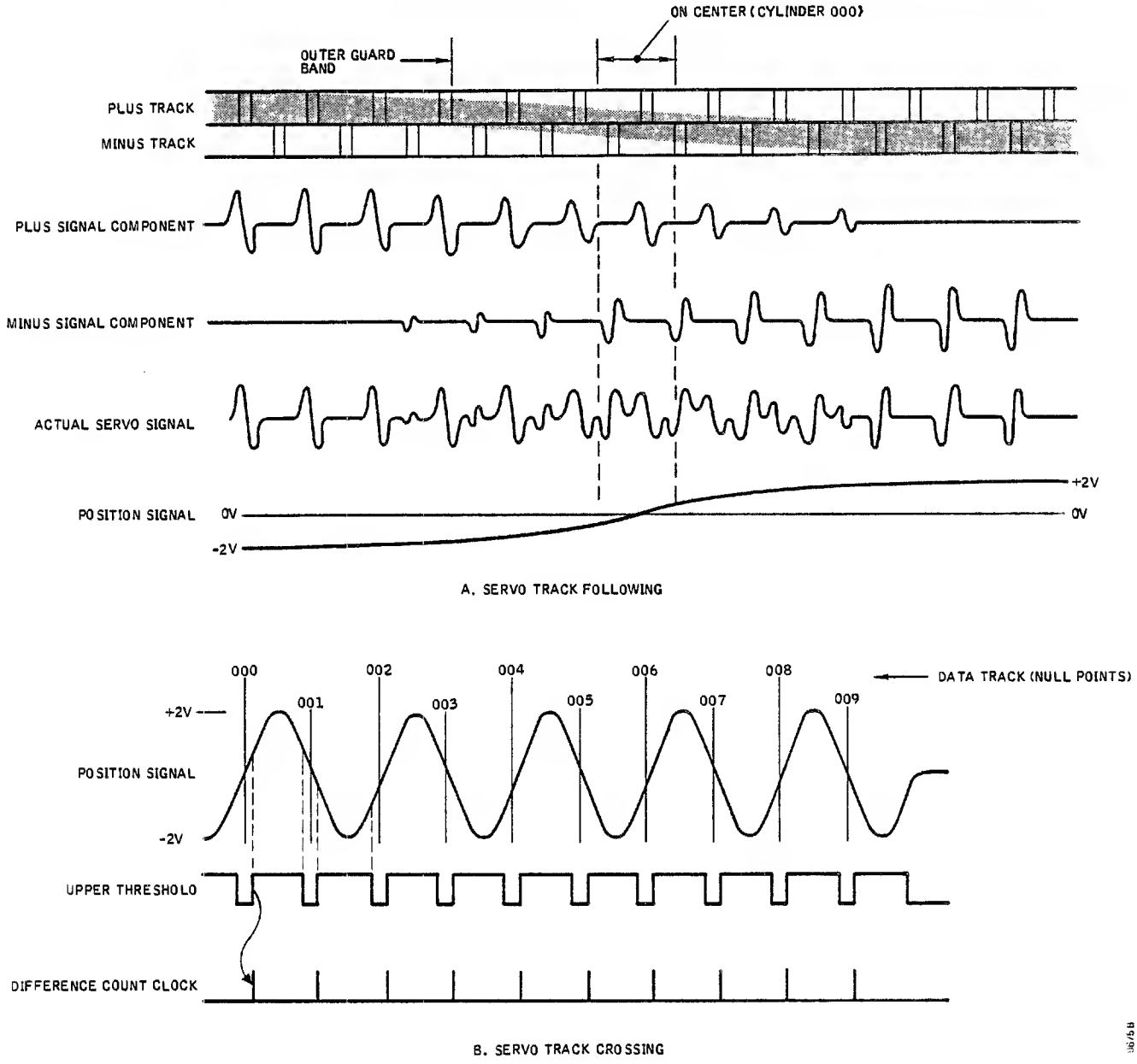

Figure 1-9. Servo System Error Positioning Signals

Any asymmetry in the dibit signal indicates that the servo head has drifted off track and produces a rising positive or negative position error signal that is applied as a correction voltage to the linear motor servo to move the servo head back to the null point of dibit symmetry.

Notice in Figure 1-9A that the position error signal can swing positive or negative by as much as 2 volts if the servo head completely loses the signal from one of the adjacent tracks. Regardless of whether the selected cylinder is odd or even, the polarity of the position signal will always be minus if the correction is toward the spindle, and positive if it is away from the spindle. The least-significant bit of the cylinder address is monitored during track following so that correction is always toward the position error null point.

One of two threshold detectors (upper or lower) is activated whenever the position error voltage indicates that the servo head is approximately 500 microinches off track. The composite output of these detectors produces a pulse train during seek-to-cylinder operations from which the decrement clock for the difference counter is derived. See Figure 1-9B. The detectors also detect off-track write operations, and produce a device check error if writing is attempted while the heads are positioned too far from track center.

A fixed forward or reverse offset of 300 microinches can be applied to the servo system under program control for attempted recovery of read data in error. Offset is produced by summing a positive or negative bias with the position error voltage.

Rezero Operation

If an illegal cylinder address is received, or if a seek-to-cylinder operation is not completed within 860 milliseconds (seek incomplete), cylinder location reference is lost. A rezero command is issued to reestablish this location reference. Rezero places the selected drive in the not-ready condition and causes a reverse seek operation that repositions the heads over cylinder 000 and resets the head address to 0. It also resets the cylinder address to 000 and resets the error condition that made rezeroing necessary.

When rezero seek operation is initiated at the rising edge of Control Tag, servo control is switched to reverse drive, load speed velocity is activated, and track following is disabled; all of which cause the linear motor to move the heads outward (with respect to the spindle) at load speed. The heads move out of the recording zone, through the outer guard band, and into the head load zone of the disk pack.

As soon as the servo head signal is lost, servo control is switched to forward mode, reversing the head drive direction. As the heads move inward, still at load speed, the servo head begins to pick up a signal again from the outer guard band. Servo control is then switched from load speed to track following and the heads continue to move inward under control of the position error voltage derived from the asymmetrical pattern recorded in the outer guard band. The servo locks in on the first dibit signal, which occurs over cylinder 000, and stops the heads on that cylinder with servo control in the track-following mode. After the rezero operation is completed, the disk drive Ready signal is available to the controller.

Head Retract Operation

A head retract operation unloads the heads from the disk pack and retracts them fully out of the disk pack area at the start of the power-down sequence or when the START/STOP switch is set to STOP. As soon as the power-on sequence or START switch signal is lost, the servo control is enabled to drive the heads in the reverse direction at load speed. This disables track following and makes the disk drive not ready.

When the heads move into the head load zone, the camming surfaces of the head arms make contact with the cam tower and force facing heads away from each other and from the disk surfaces. The heads continue to move outward toward the linear motor; this causes the carriage to open the Heads-Extended microswitch.

This action disables the positioning servo and permits the solid-state relay to remove ac power from the spindle motor. A braking circuit is activated that applies a 50-volt dc braking voltage to the eddy current brake for approximately 18 seconds. The disk pack should come to a complete stop during this period to complete the power-down sequence.

Data Recording Method

Triple Frequency Modulation (TFM) is the recording method used in the Trident Disk Drive. Figure 1-10 provides a comparison between NRZ (non-return-to-zero) and TFM data. TFM is so called because flux reversals on the recording media occur at three frequencies: at one, one and one-half, and two-bit cell intervals. This method of recording has three major advantages:

- Fewer flux reversals (lower recording frequency) for a given amount of data in a self-clocking scheme, permitting a higher packing density
- Contains data bit and clock information, both of which are recoverable
- Flux change polarity has no relationship to bit value, simplifying data recovery circuit design

Data cell time for the 4040 bpi packing density of the T200 disk drive is 155 nanoseconds at speed, making the maximum recording frequency 6.4 megahertz (all-zeros or all-ones bit pattern). Minimum recording frequency is half that, or 3.2 megahertz (for alternate zero and one bit pattern).

Data cell time for the 6060 bpi packing density of the T300 disk drive is 103.3 nanoseconds at speed, making

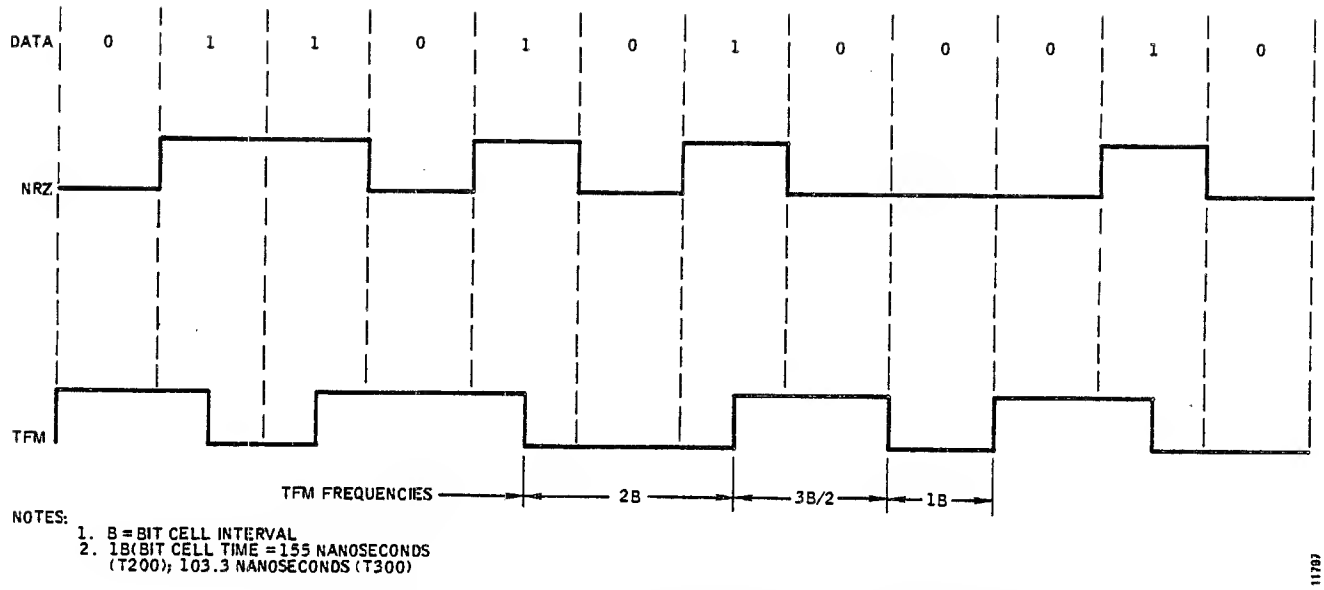

Figure 1-10. Code Format Comparisons and TFM Characteristics

the maximum recording frequency 9.67 megahertz (all-zeros or all-ones bit pattern). Minimum recording frequency is half that, or 4.84 megahertz (for alternate zero and one bit pattern).

TFM coding can be simplified to the following three rules:

- A flux change occurring at the midpoint of a data cell is a one data bit, regardless of polarity
- A flux change occurring at a data cell boundary is a data clock, regardless of polarity
- A data clock flux reversal can only (and will always) occur between two zero bit data cells

TFM data and clock information is recovered during reading by establishing bit cell time-related detection windows. This is explained in greater detail under Read Data Recovery.

Peak Shift Precompensation

High-density, multifrequency recorded signals suffer from a magnetic effect known as peak shifting. Peak shifting is the tendency of closely spaced flux reversal domains to migrate away from each other into areas of lower density. In effect, unevenly spaced flux reversals stress themselves in an attempt to even out the spacing between them. See Figure 1-11.

This magnetic interference effect, if not compensated for, could cause data and clock recovery problems during reading if detection window timing is marginal. To minimize the effect, the data is written in a prestressed condition. That is, flux reversals that would tend to be shifted late due to magnetic interference are written early, and vice versa (T300 only).

In the T300 drive, prestress direction is determined automatically in the following manner; the incoming synchronized data train is broken up in increments of five bits. This five-bit pattern addresses a PROM that itself contains addresses of pre-determined delay times to match any possible data pattern. Time delays are actually selected from a tapped data line. This process is repeated for each bit in the data train.

Write Data Recording

Data to be written on the disk pack is sent by the controller in the form of serial NRZ code synchronized to a bit-rate write clock provided by the disk drive. This clock is derived from a phase-locked oscillator that is locked onto the servo head dibit signal.

The head to be used for writing must be addressed prior to the actual write operation. This is done by presenting the binary head address (0 thru 18) on the Bus lines and raising the Set Head Tag while the drive is selected.

Note

Actual writing of records requires pack initialization and sector identification read operations that are beyond the scope of this discussion. Refer to the OEM Reference Manual for information regarding sectoring operations and sector format descriptions.

Selection of the head addressed is executed by setting the Head Select line high and raising the Control Tag line. This bit must be active for a predetermined time before the read or write command is given and must remain active to keep the head selected.

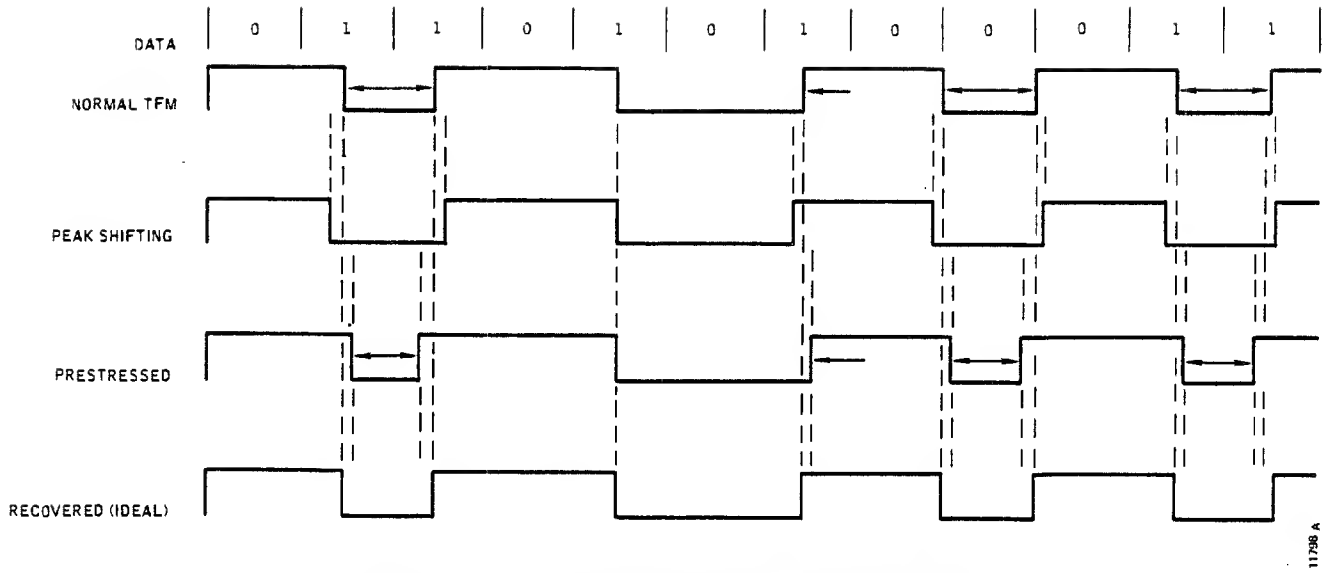

Figure 1-11. Effects of Peak Shifting and Prestressing

The write command is issued while the Control Tag and Head Select lines are high. This turns on the write circuits of the selected head. NRZ data on the read/write data lines is clocked into a NRZ-to Miller Code converter by the same bit-rate clock supplied to the controller for strobing out the write data. Synchronous Miller code data from the converter pass to precompensation logic where the decision is made to clock each pulse on time, early, or late, as discussed earlier.

The precompensated code is the clock that toggles a flip-flop; the output of this flip-flop directly controls flux reversals of the write current driver for the selected head.

Address marks (for variable-length sectoring) are commanded to be written during pack initialization while writing is enabled (Control Tag, Head Select, and Write lines are high). This address mark line must remain high for 6 to 8 microseconds to start an interval during which flux transitions are inhibited. This produces an address mark of three bytes without flux reversals, which is readily identifiable when searching for the start of a sector — a read operation.

The write current to the selected head is not constant but is reduced in seven step increments as the heads move inward toward the hub. This is necessary because the peripheral velocity of the pack decreases closer to the hub so that air barrier pressure decreases, making the heads fly closer to the disk surface. If the write current were not reduced when writing on inner cylinders, flux saturation would occur; this would reduce frequency response and increase crosstalk between tracks.

Read Data Recovery

Data read from the disk pack is sent to the controller in the form of serial NRZ code accompanied by a bit rate-read clock provided by the disk drive for data strobing. This clock is derived from a phase-locked oscillator that is locked onto the data stream from the read/write head.

The head to be used for reading must be addressed prior to the actual read operation in the same manner as for writing. Refer to the Write Data Recording discussion.

Accuracy of data recovery depends upon setting up accurate strobe windows relative to the raw data being read. This is accomplished by synchronizing a phase-locked, voltage-controlled oscillator (VCO) with the clock transitions of the read signal. This oscillator has an operating frequency that is twice the bit interval rate (2F or 12.9 megahertz, T200; 2F or 19.34 megahertz, T300). This rate is divided down to produce the bit rate frequency (F for T200 = 6.45 megahertz; F for T300 = 9.67 megahertz).

The series of known all-zero bytes in the preamble of the record produces a TFM high-frequency pattern at the bit rate (F). These are used for initial synchronization by making a phase comparison between them and the divided output of the VCO. Phase differences produce a correction voltage that changes the VCO frequency until the oscillator is captured and locked in phase with all-zero bit rate clocks.

The raw read signal from the selected head is amplified and processed into a digital stream of clock and data pulses. Detection windows are set up by the F and F/ timing signals that are phase-shifted 90 degrees relative to the bit time interval. See Figure 1-12. Read pulses that rise within the first or last ¼ sectors (F/ true time) of the bit time interval are detected as clock pulses. Read pulses that occur within the middle ½ (F true time) sector of the bit time interval are detected as binary 1 data pulses. Notice that jitter due to peak shifting of the read pulses will not affect accurate data detection, so long as it occurs within the middle ½ sector of the bit interval.

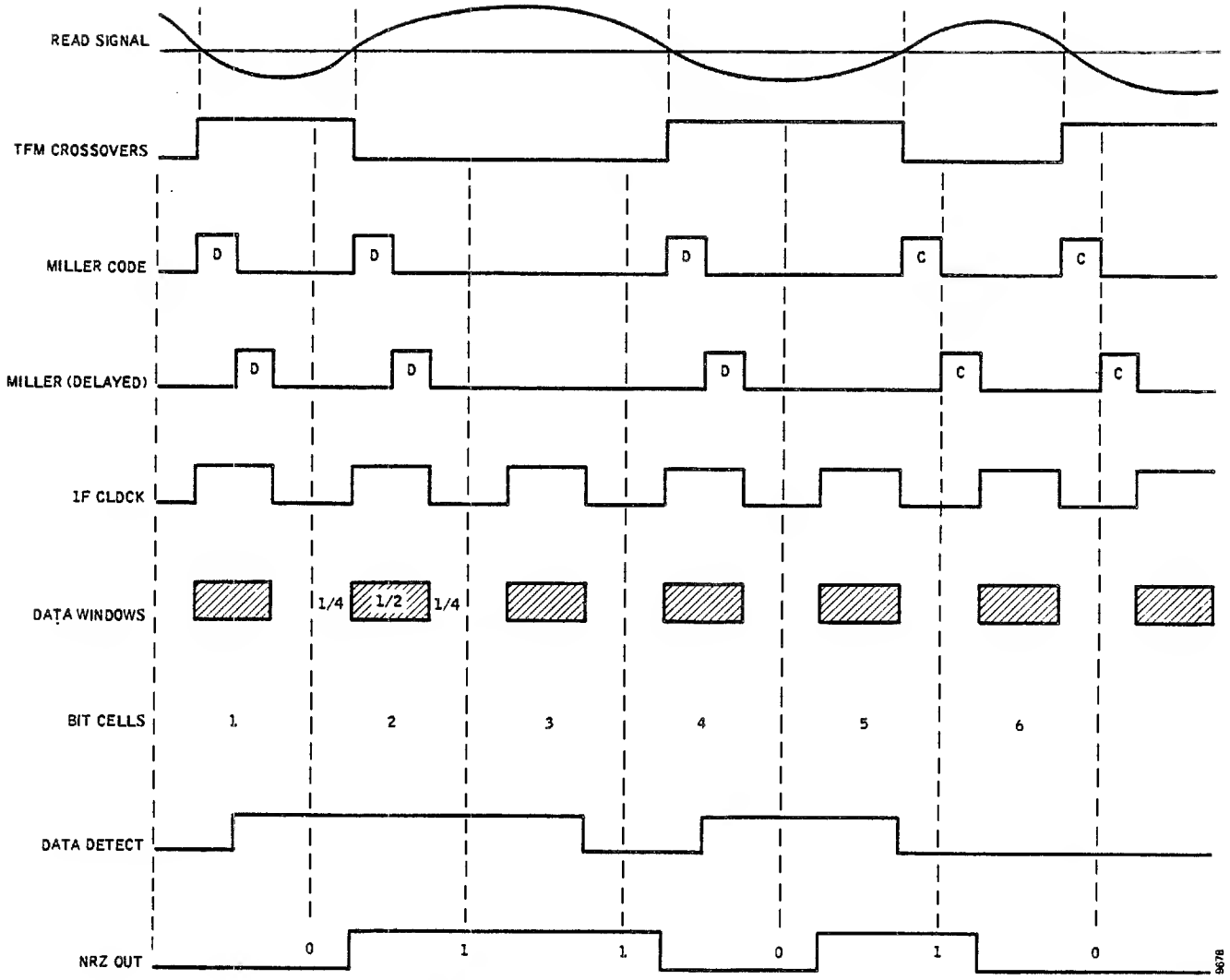

Figure 1-12. Read Data Detection

Detected data is converted to bit-interval synchronous serial NRZ code and sent to the controller.

If the read pulses occur marginally out of time with the read detector windows for accurate data recovery, the windows can be strobed early or late under program control while reading. This skews the delayed data one way or the other by a few nanoseconds relative to the window.

When the address mark detector is activated during reading, it monitors the read pulse stream. If a read clock or a data pulse does not occur within 1.8 microseconds, an Address Mark Detected signal will be sent back to the controller. Address marks are used on a variable length sectored pack and signal the start of each sector.

Read-only operations are normally terminated by dropping the Read Gate signal. However, if reading is being done for track and sector location prior to a write operation, the read operation is terminated by dropping the Read Gate signal and raising the Write Gate signal (Control Tag and Head Select lines remain high) after an appropriate delay.

Fixed-Length Sectoring

A hardware counter in the disk drive produces pack synchronous sector pulses. These pulses are carried on a Selected Sector line in the bused cable and on a Composite Sector/Index line in the radial cable from each disk drive when the heads are loaded.

The sector counter defines the sector length (and therefore the number of sectors/track) by counting at the dibit rate.

The number of bytes per sector is selected by jumper connections that preload a byte count into the counter. This byte count can be any number greater than header plus overhead bytes up to a maximum of 6142 bytes (T300) or 4095 bytes (T200).

The index pulse and each sector pulse preload the sector counter with the jumper-selected bytes-per-sector count.

This count is counted down by a 806 kilohertz (at speed) signal derived from the servo head dibit signal. Each count represents 1 byte (T200) or 1½ bytes (T300).

When the count has been reduced to zero, a sector pulse is generated for 1.24 microseconds at speed, and the counter is reloaded for the next sector count. See Figure 1-13.

Index markers are detected from the servo head dibit signal by a separate circuit and produce a 4-microsecond pulse on a Selected Index line and on the Composite Sector/Index line. This circuit detects the index pattern of the three lost dibits that have been prerecorded on all servo tracks.

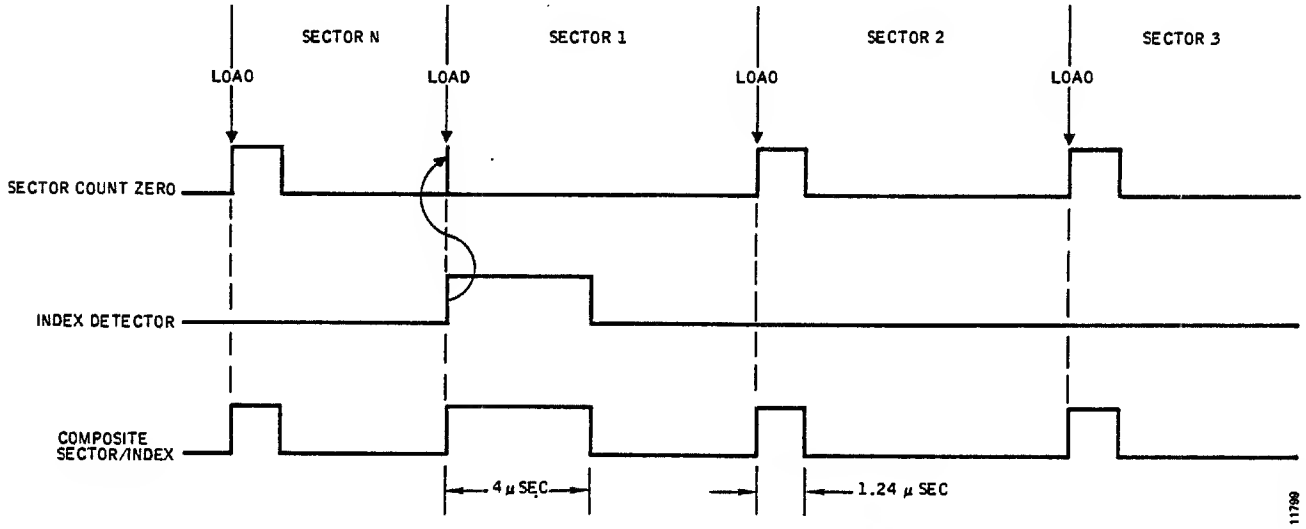

Figure 1-13. Composite Sector and Index Signal

SECTION 2
POWER SEQUENCING

Power sequencing is a function of the Disk Pack Drive System (see Figure 2-1). This system controls the application of power to the spindle motor and to the eddy current brake. It also initiates first-seek and head-retract operations that are part of power-up and power-down sequences.

POWER TURN-ON

Power is applied to the disk drive through Circuit Breaker CB1 located on the Ac Distribution Box Assembly. Turning on this breaker activates the blower motor, energizes the dc power supply, and provids ac power to the spindle motor sequencing relay. A 1.0- to 7.0 second power initialize (PWRINI) pulse is produced when the output of +5-volt power supply goes high. This pulse operates as a general system reset pulse, which ensures that all critical control flip-flops and counters are set or reset to initial states.

The occurrence of PWRINI also starts a braking period of approximately 11 seconds to ensure that power-up sequencing begins with the spindle stopped. Power-up sequencing of the disk drive is inhibited until this braking period times out. The logic that performs this function is the Sequence Control Logic and is described in a subsequent discussion.

When power turn-on is complete, the blower motor will be operating, the dc power supply and all disk drive logic circuits will be active, and the spindle drive motor will be stopped. This is the normal standby state. The disk drive will still be offline to the controller if the front panel START/STOP switch is set to STOP.

SEQUENCE OSCILLATOR

Clock signals for timing and control of the sequence control logic and a portion of the status logic are derived by dividing down the 12.6KHZOSC output from the Head-Positioning Servo System. This signal is in turn derived from the Phase-Locked Oscillator (PLO), which operates as a free-running oscillator when power is turned on and the heads are not

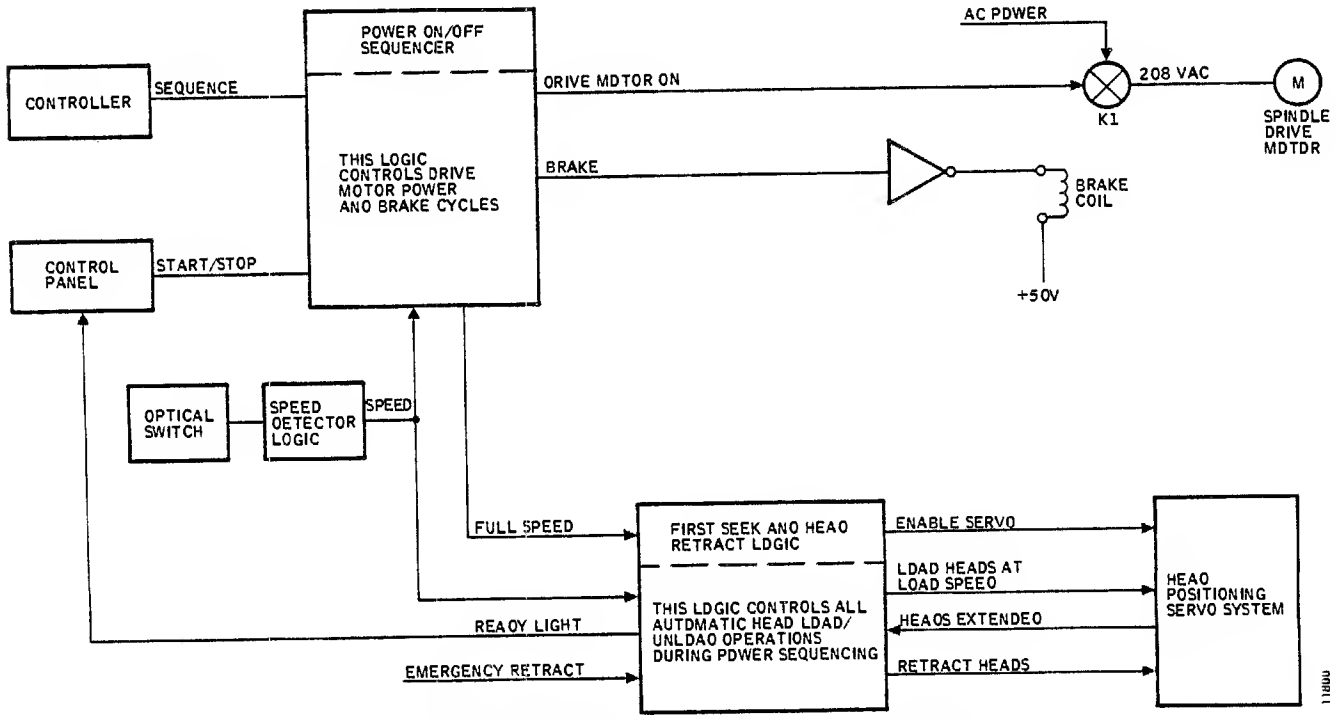

Figure 2-1. Disk Pack Drive System, Block Diagram

loaded. PLO frequency differences, when locked to the servo head signal and when free-running, are adjusted to be negligible.

Division of the 12.6KHZOSC pulse train into clock pulse trains of the desired frequency is done by a modulo 16K counter (Figure 2-2). The following clocks are detected:

- 1.3SOSC
- 650MSOSC
- 325MSOSC
- 82MSOSC
- 0.32MSOSC
- 0.16MSOSC

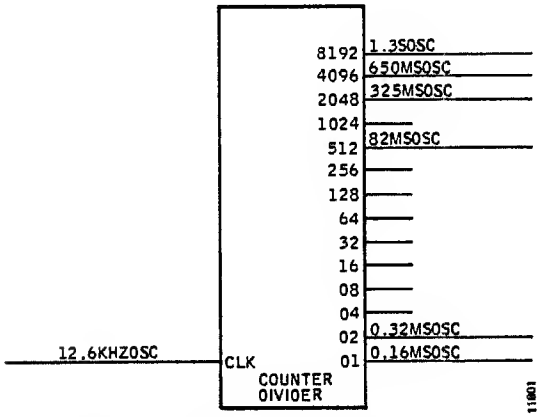

Figure 2-2. Sequence Oscillator Counter

The 1.3SOSC, 650MSOSC, and 325MSOSC clocks are used by the Sequencing Control Logic to time power-up and power-down sequencing operations. The 82-, 0.32-, and 0.16-millisecond oscillators are used in the status logic to time seek incomplete, head loaded delay, and track-following delay operations, respectively.

SEQUENCE CONTROL LOGIC

The sequence control logic incorporates the following major functional elements (Figure 2-3):

- Spindle drive motor logic
- Sequence counter and associated timing logic
- Pack-on flip-flop
- Spindle brake control logic
- Head position control flip-flop

When the sequence signal from the controller is presented to the drive interface, the spindle drive motor logic generates the drive motor control signal. In single drive systems, the START/STOP switch can perform the same function when the sequence signal is present. The drive motor signal starts (or stops) the drive motor and controls the up or down count direction of the sequence counter.

The sequence counter and associated timing logic time the drive motor startup, establish a time window to determine whether or not a pack is mounted, command head load and retract operations, and control the spindle brake under normal conditions.

Should an attempt be made to start the drive with no pack installed, the pack-on flip-flop detects this occurrence by looking at the disk speed through a timing window. An excessive rise in speed indicates that the disk pack has not been mounted, and the pack-on flip-flop initiates a brake cycle to stop the disk.

During normal operations, brake cycles are initiated by the sequence counter and implemented by the brake control logic. The exception to this was noted in the previous paragraph. When the brake logic is active, the drive motor logic is inhibited.

The head position control flip-flop generates the signal that allows the head-positioning system to load or unload the heads from the disk pack. During a power-up sequence, it enables head loading after a delay of approximately 20 seconds; when a power down sequence is initiated, the heads are retracted immediately.

Power-Up Sequence

When the dc power in the drive comes up, the logic is initialized and PWRINI (Figure 2-4) loads the Sequence Counter with a count of eight (decimal). Since DRMOT/ controls the count direction, the counter is initially set for a down-count operation. With the counter output at any count other than zero or full count (15 decimal), FULLSPEED is low and the counter is enabled for operation at a 1.3-second clock rate. FULLSPEED and DRMOT/ generate the BRAKE signal, which inhibits the drive motor enabling gate and energizes the brake coil. This condition exists for approximately 11 seconds while the counter counts down to zero.

FULLSPEED goes high when the count reaches zero, thereby freezing the counter and releasing the disk brake. BRAKE/ releases the drive motor enabling gate for operation at this time. The gate is made by either the SEQUENCE signal or the START LTH signal, depending upon the operating system, and the drive motor flip-flop sets. This action reverses the direction input to the sequence counter to initiate an up-count operation, and picks the solid-state switch that controls ac power to the spindle drive motor.

As the drive motor begins turning and the up-count progresses, the speed detector begins picking up pulses from an optically sensed pattern of notches on the spindle brake disk. At the count of 2.5, the state of the SPEED signal is monitored. With no pack mounted, the SPEED signal will prevent the pack-on flip-flop from setting; SPEED and PACK ON/ then set the No Pack Brake Latch, thereby initiating a brake cycle and removing power to the drive motor.

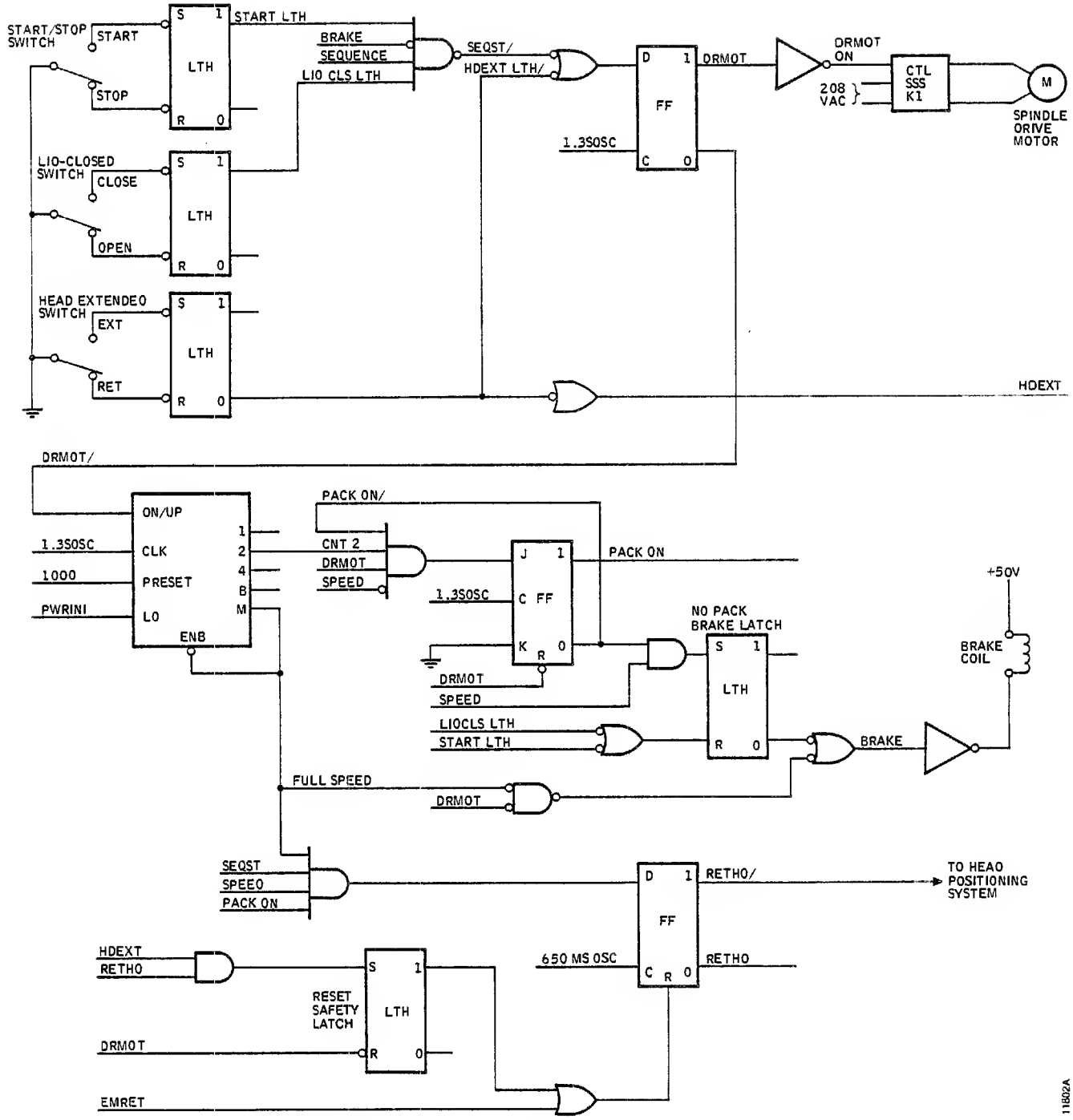

Figure 2-3. Power Sequencing Logic, Simplified

At the count of 2, SPEED is normally inactive and the pack on flip-flop sets. As the count progresses SPEED becomes active and, when the counter counts out, FULLSPEED again goes active, and locks up the counter.

The previously conditioned enabling gate that sets the retract heads flip-flop is made when FULLSPEED comes up, and RETHD/ goes high on the clock. RETHD/ enables the head-positioning system to allow the servo control logic to initiate the first-seek operation. The complete power-up sequence requires approximately 20 seconds.

Power-Down Sequence

During a controller-initiated power-down sequence, the SEQUENCE input is dropped, causing the drive motor flip-flop to reset. When the operator initiates the sequence, START LTH falls, which effects the same result.

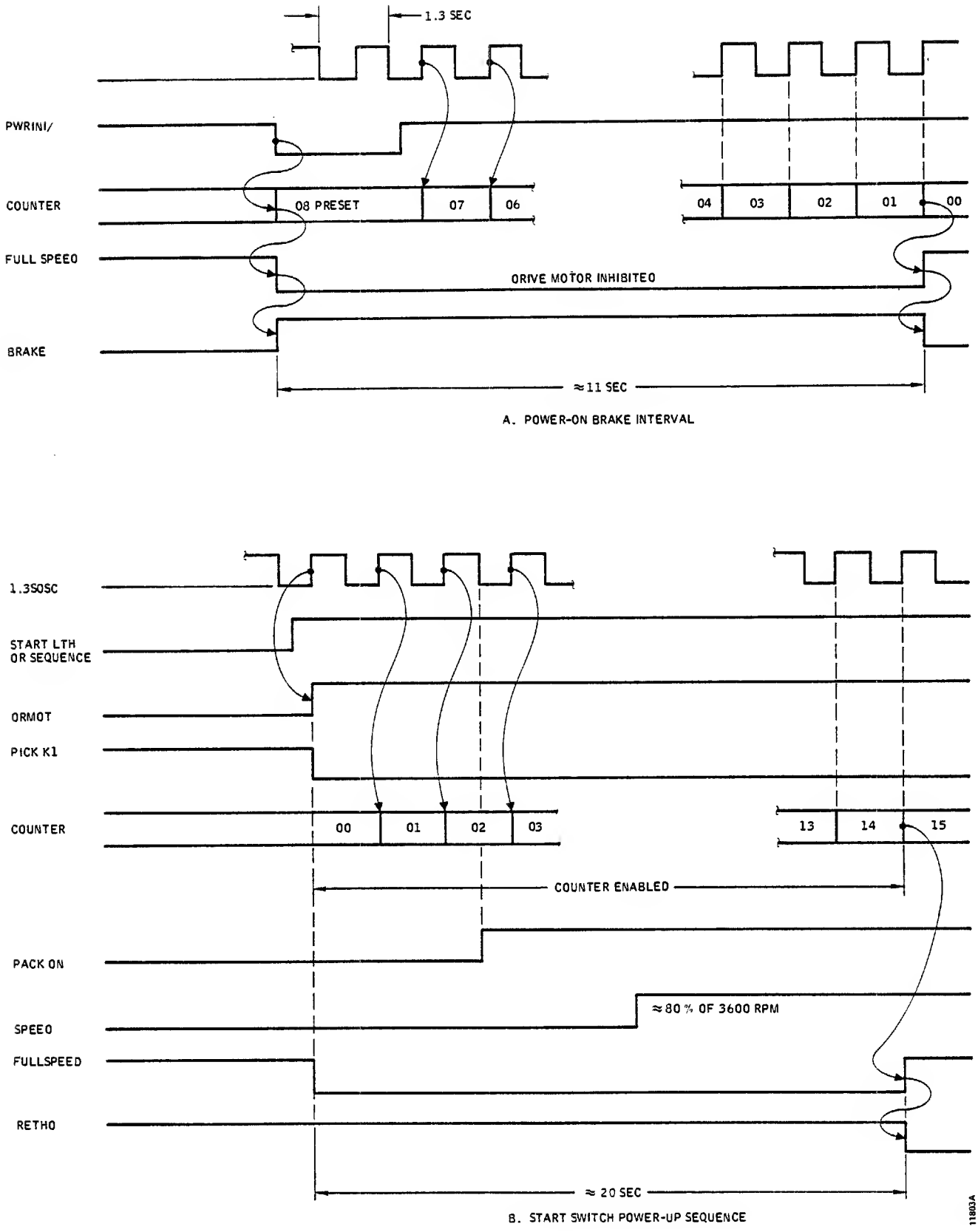

Figure 2-4. Power-Up Sequence Timing Diagram

Losing SEQST causes RETHD/ to fall (Figure 2-5) and the servo control logic begins the head retract operation. After the heads are in the hole, HDEXT LTH becomes inactive and, in conjunction with the false SEQST signal, resets the drive motor flip-flop. DRMOT drops K1, and the spindle drive motor begins to slow down.

At the end of the count-up sequence, the sequence counter is disabled with a full count of 15. When the drive motor flip-flop resets, the counter is set for a down-count operation that begins immediately. With FULLSPEED and DRMOT both inactive, a brake cycle is initiated and the disk pack is brought to a complete stop in approximately 20 seconds.

An unscheduled power-down sequence can take place if the disk speed should fall to an unsafe level, or if an emergency retract occurs. The loss of SPEED resets the retract heads flip-flop through the enabling gate to the flip-flop, while the emergency retract (EMRET) signal resets the flip-flop directly. In either case, the heads retract and the pack continues to spin.

A reset safety latch is set when the heads are extended and the retract head flip-flop is reset indirectly. The latch applies a direct reset to the flip-flop, and holds the flip-flop reset until the heads are in the hole.

SPEED DETECTION

Detecting the rotational speed of the disk pack is accomplished by optically sensing a pattern of notches that are machined into the edge of the brake disk. Actually there are two identical patterns 180 degrees apart (to ensure reliability), but only one pattern is necessary in the detection scheme employed. The basic elements of the detection circuit are an optical switch and two one-shots (Figure 2-6).

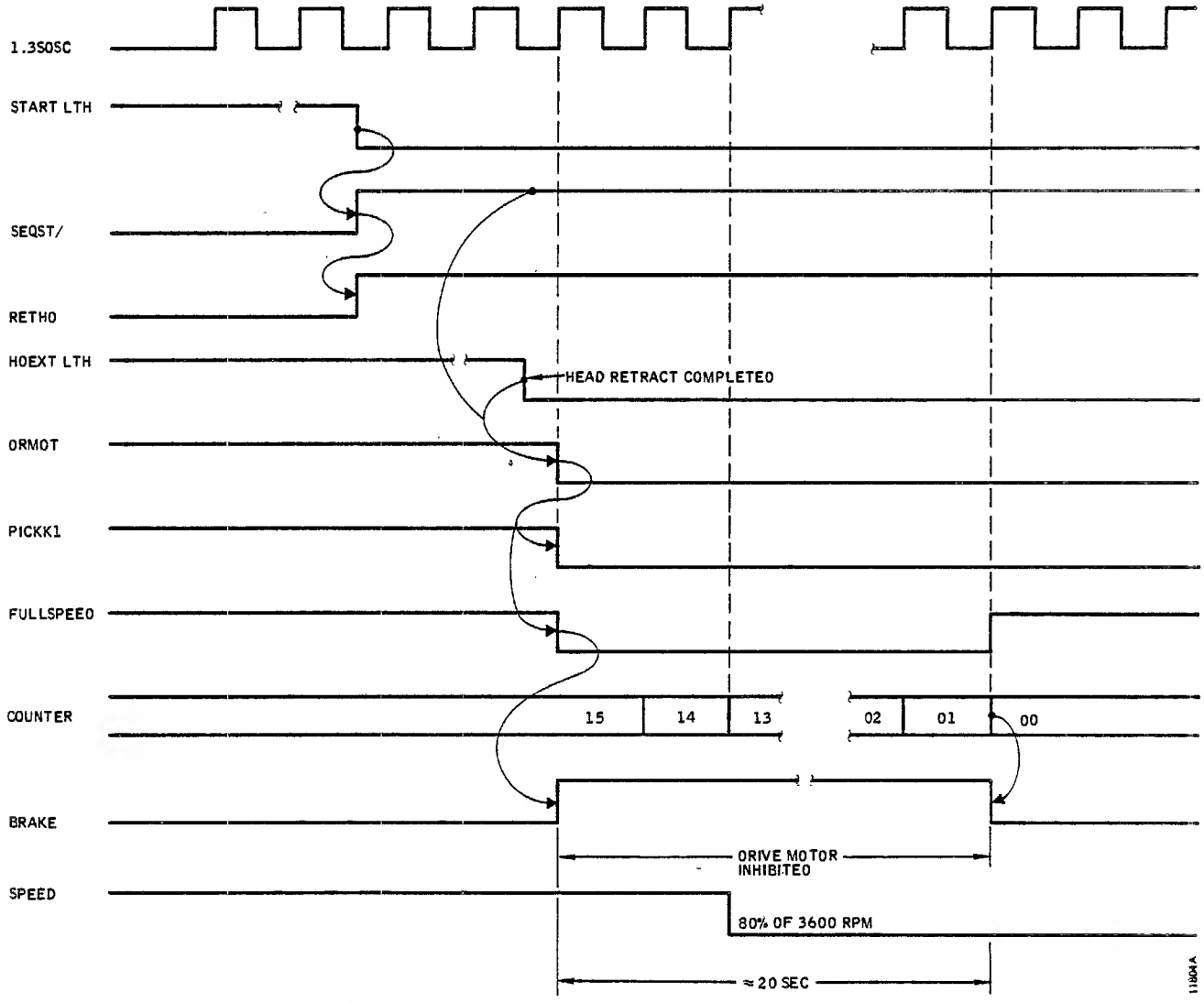

Figure 2-5. Power-Down Sequence Timing Diagram

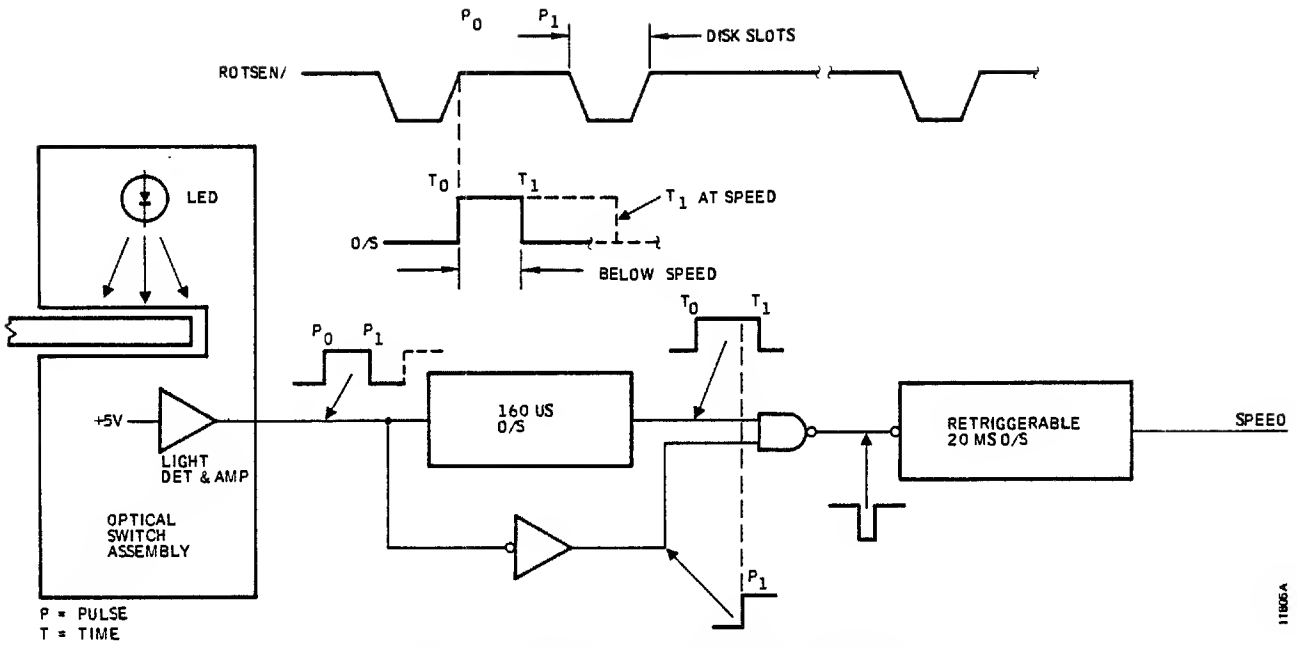

Figure 2-6. Speed Detection Logic, Simplified

As a notch moves under the LED the light detector in the optical switch senses the light output of the LED and produces a pulse. This pulse triggers a one-shot that has an output pulse duration of 160 microseconds. The inverted output pulse of the switch is NANDed with the 160-microsecond one-shot output.

While the disk speed is building, the duration of the switch output pulse exceeds the 160-microsecond one-shot pulse duration. and the gate output remains high. The 20-millisecond one-shot is not triggered, and SPEED remains inactive.

When the disk speed increases to a point (80 percent of full speed or approximately 2880 rpm) where the switch output pulse duration is less than the 160-mircrosecond one-shot pulse duration, the NAND gate produces a negative-going pulse that triggers the 20-millisecond one-shot. and SPEED goes active. Once the speed is up, this one-shot is retriggered continually, and SPEED stays active.

The disk speed varies somewhat due to power fluctuations and, when this happens, the inertia of the disk pack prevents instantaneous changes. Actually, one revolution of the pack at full speed corresponds to approximately 16.6 milliseconds. The 20-millisecond one-shot duration allows a time compensation for the second set of pulses to be detected so that a loss in disk speed will not be falsely indicated.

SEQUENCE-IN-PROCESS INDICATION

The green Ready indicator on the operator control panel flashes during power-up and power-down sequences. Flashing occurs at the 1.3-second rate of 1.3 SOSC clock signal. There are two functional control gates. See Figure 2-7.

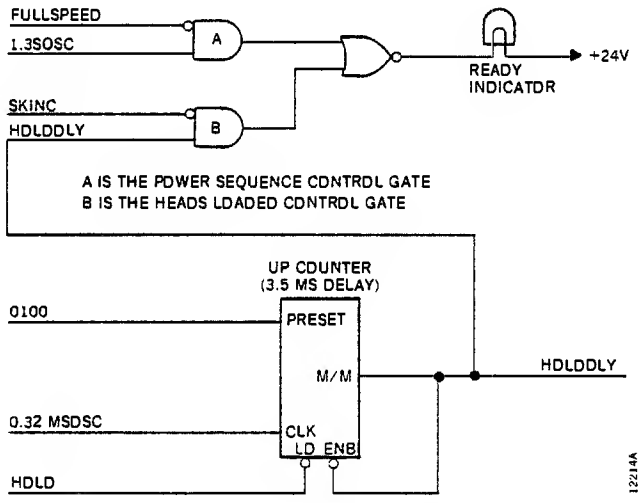

Figure 2-7. Drive Ready Indicator Logic

The Power Sequence Control gate controls the operation of the Ready indicator during power sequencing operations. This gate is enabled and disabled according to the clock state during either power-up or power-down sequencing. When FULLSPEED goes active, control of the Ready indicator is assumed by the Heads Loaded Control gate.

When the servo head begins picking up recorded tracks on the outer guard band HDLD (heads loaded) goes active and releases the load input to a 3.5 millisecond delay counter. This counter produces HDLDDLY (heads loaded delay). The Heads Loaded Control gate generates the active signal that holds the indicator on as long as the heads are loaded and a seek incomplete does not occur.

When a power-down sequence is initiated FULLSPEED goes inactive and the Power Sequence Control gate assumes control of the Ready indicator. After the brake cycle is complete (approximately 20 seconds) FULLSPEED goes high and the indicator goes out.

SECTION 3
INTERFACE AND CONTROL

This system receives command inputs from the controller via select, bus, and tag lines and translates the commands issued over these lines into drive control signals required for their execution by the other systems. When the disk drive is offline, the controller interface is disabled, and equivalent parallel inputs from the T2000B Exerciser will be accepted and executed for offline maintenance operation.

The output interface counterpart of this system, which reports disk drive operational and error status, is described in Section 6.

INPUT INTERFACE SIGNALS

Table 3-1 lists and defines all signals to the Input Interface and Control System from the controller. These signals are carried by single-ended, twisted-pair lines in the radial and bused cables to the drive. These lines are terminated by 100 ohms and +5 volts at both ends. All signals, except controller terminator power, are low-level true, with high level being defined as 5.0 ±0.5 volts and low level as 0.2 +0.2 volts. Dual-access units accept two identical sets of signals.

SYSTEM OPERATION

Figure 3-1 shows the primary components of the Input Interface and Control system as described in this section. These include:

- Drive Selection Logic
- Cylinder Address Register
- Head Address Register
- Control Command Decoder
- Index Detector
- Sector Counter

Drive selection logic monitors the radial cable Select signal. If the disk drive has not been placed offline by the Degate switch, the selected condition is propagated to the Control Command Decoder and to the other disk drive systems. A selected signal is returned to the controller to indicate that the drive has accepted the Select signal addressing it (i.e., the drive is not offline).

The Control Command Decoder gates bus line commands to the other drive systems when the drive has been selected and while the Control Tag line is active.

Offset on/off commands are also received and stored by the section when the Set Head Tag line is activated.

A 10-bit Cylinder Address Register holds the cylinder address of the current head position. This register is reset to zero by a first-seek operation and whenever a rezero command is received and executed. The Head Positioning Servo System uses this current cylinder address to calculate the difference, in number of cylinders, between the current head position and the new cylinder address placed on the bus lines when the Set Cylinder Tag line is active. After the difference count is calculated and stored, the bus line address is loaded into the Cylinder Address Register as the new current address. Dropping the Set Cylinder Tag line signal initiates the seek operation to the new cylinder position. If the address on the bus lines is greater than 814, an Illegal Cylinder condition is detected. This is a Device Check condition that inhibits execution of the seek operation.

The Head Address Register stores a head address presented on the bus lines when the Set Head Tag line is activated. This register can be parallel-loaded, its address advanced by successive Head Advance control commands, or reset to the Head 0 address by an HAR Reset command. Status signal End of Cylinder becomes active when the Head Address is set or advanced to a head address greater than 18. The direction of an offset operation is also stored in the Head Address Register.

An Index Detector monitors servo-derived GAPCLK pulses from the Head-Positioning Servo System. A pattern of three lost dibit pulses is recorded on all servo tracks to mark the starting point of each cylinder (index). The Index Dector produces a 4-microsecond Index marker pulse each time this pattern is detected, which is sent to the controller as status.

A fixed-length Sector Counter produces a 1.24-microsecond sector marker pulse whenever its count is reduced to zero by 806 kHz clock pulses from the Head Positioning Servo System. The preset count of this counter is jumper selectable, allowing the user to choose any sector length up to 6142 (T300) or 4095 (T200). Every time a sector marker pulse is produced and sent to the controller as status, the Sector Counter is reloaded to the count selected by the preset jumpers to start the next sector count. The Index marker also presets the counter, establishing sector synchronization with the start point of each cylinder.

TABLE 3-1. INPUT INTERFACE SIGNALS

Signal Name	Functional Description
	Radial Cable
ISEQUENCE/	A low level on this line initiates power-up sequencing and holds the drive in the power-up state. A high level initiates power-down sequencing and holds the drive powered down.
ISELECT/	A low level on this line selects the drive to receive bused cable commands and to send and receive read/write data. A high level deselects the drive.
CNTLRP5V	Controller +5v for signal terminator power.
AREQUEST/ BREQUEST/	Dual access drives only. Request signals enable dual-access control logic so that the drive may be selected by the controller. Low level is the active state.
	Bused Cable
IBUS0 thru IBUS9/	Ten bus lines over which the controller sends cylinder addresses, head addresses, and operating commands. Data on these lines must be active at least 200 nanoseconds before and after a tag line is active.
ISETCYLTAG/	Set cylinder tag line that causes the selected drive to accept bus line data as a new cylinder address. A low level on this line loads bus data into the Cylinder Address Register. The high-level trailing edge initiates the seek operation to the new cylinder.
ISETHDTAG/	Set head tag line that causes the selected drive to accept either or both a new head address and head offset command on bus lines. A low level on this line loads the Head Address and Offset Registers.
ICONTROLTAG/	Control tag line that causes the selected drive to decode bus line data as control commands. Low level is the active state.

ONLINE/OFFLINE CONTROL

The online/offline status of the drive is controlled by the setting of the Interface/Degate switch (see Figure 3-2). When the switch is set to the ONLINE position, the I/O Control Latch is set and the interface is controlled by the controller. When the switch is set to OFFLINE, the latch is reset, the drive is controlled with the exerciser, and the signals shown perform the following functions:

- I/O ENABLED/ generates an active UNTSEQ signal that initiates a power up sequence under control of the START/STOP switch located on the operator control panel.
- DEGATE/ indirectly disables the input interface and directly disables the greater portion of the output interface (Refer to Section 6 for details on the output interface).

The I/O ENABLED term is used on dual access machines only. Its function is covered in the discussion subtitled Manual Control Logic under the title heading Dual Access Control contained in this section.

DRIVE ACCESS CONTROL

All controller-initiated power sequencing and disk drive selection operations are handled over the radial cables lines, effectively slaving each disk drive to the physical address assigned to the radial cable connected to it. Consequently, no physical address plugs or other unit-addressing logic are incorporated in the design of these drives.

Typically, the controller initiates the disk drive power-up sequence and then issues a drive select command to see if the drive is selected (not offline). When the disk drive is powered up and ready to accept controller commands, the drive sends an attention signal to the controller, whether the drive is selected or not. The controller must select the drive in order for the drive to respond to any operational commands or to present status over the bused cables. All drive system bused cables, bused cable terminator, and controller terminator power (+5v) must be present for drive access.

Figure 3-3 is a flow diagram of disk drive responses to controller sequencing and select commands.

DRIVE SELECTION LOGIC (SINGLE ACCESS)

The drive selection logic differs depending upon whether or not the drive is a single- or dual-access unit. Simplified single-access drive selection logic is shown in Figure 3-4.

The UNT SEQ line that enables power-up sequencing and power application to the Spindle Drive System is active under two conditions:

- ISEQUENCE and ITERM+5V signals from the controller are high. This is the normal online condition.
- The Interface/Degate switch is in the OFFLINE position. This is the degated or checkout condition.

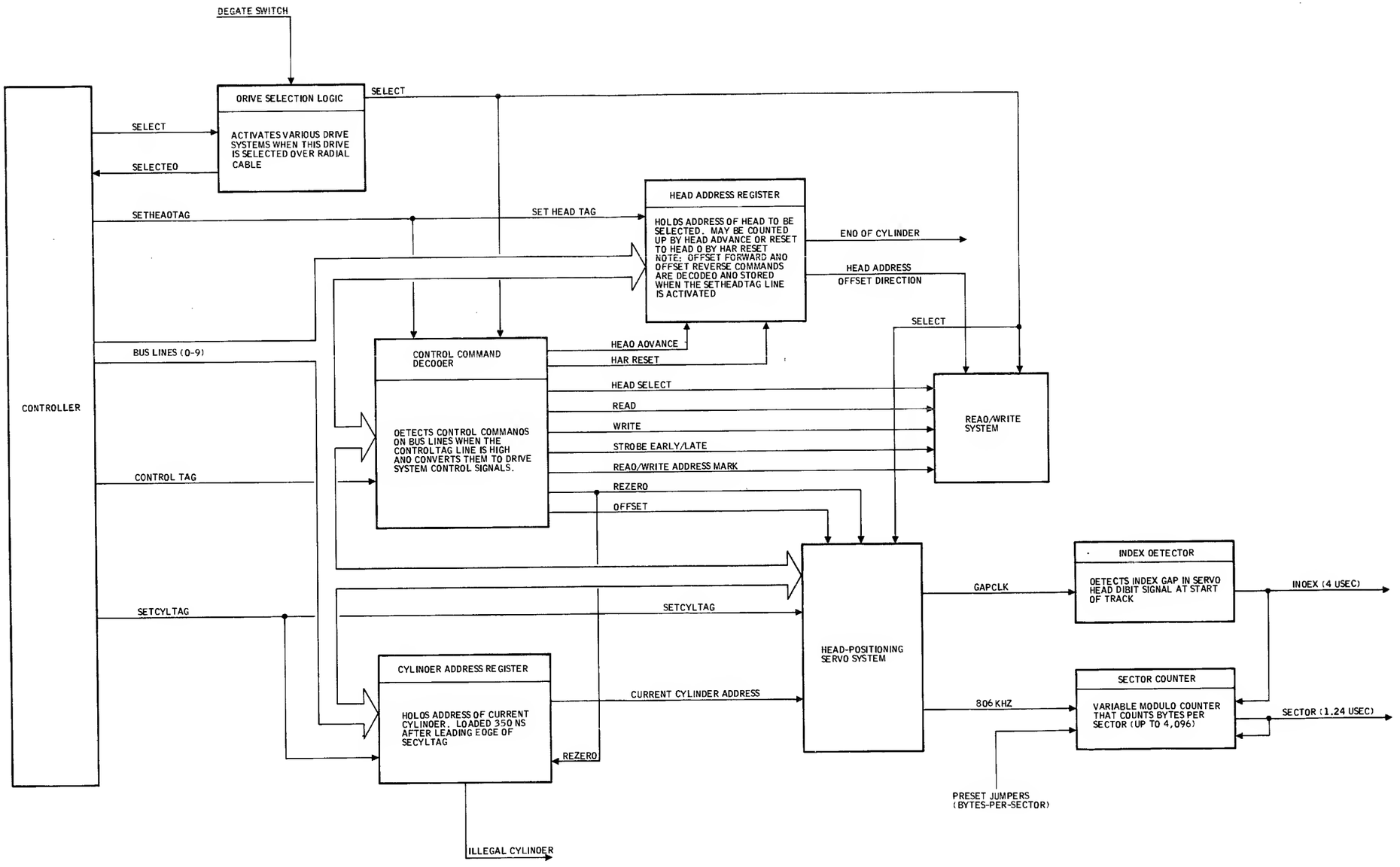

Figure 3-1. Interface and Control System, Block Diagram

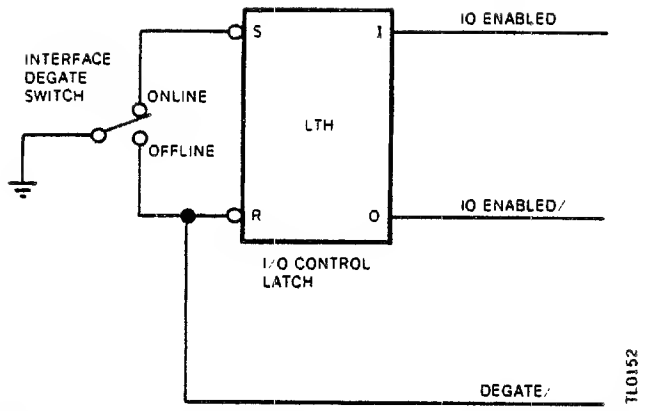

Figure 3-2. Online/Offline Control Logic, Simplified

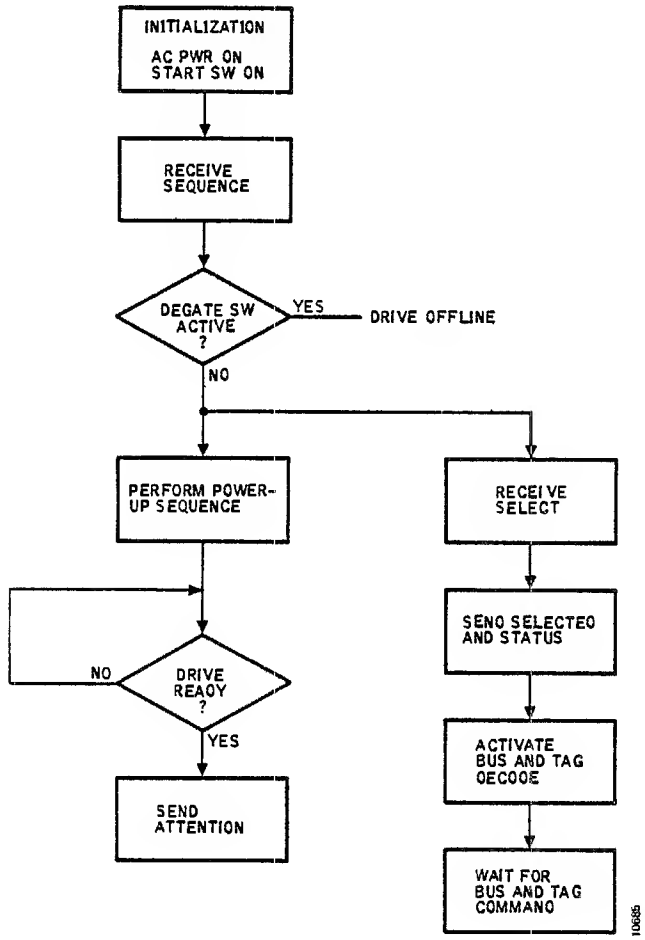

Figure 3-3. Drive Access Control, Flow Diagram

In either of the above cases, the sequence logic is enabled for operation. The former case allows automatic power sequencing while the latter requires a manual operation. Refer to Section 2 for details on power sequencing.

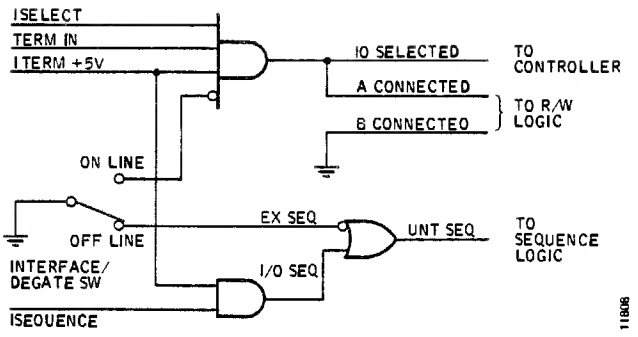

Figure 3-4. Single Access Drive Selection Logic, Simplified

Online drive selection requires the Interface/Degate switch to be set to online and the bused cable terminator to be installed (TERMIN). With these conditions true, each time the controller makes the ISELECT line active, the IOSELECTED return line to the controller is activated. Notice that setting the Interface/Degate switch to OFFLINE also generates the UNTSEQ signal necessary for offline operation of the drive by an exerciser.

The A CONNECTED, B CONNECTED lines are routed to the read/write logic. Grounding the latter line simply disables the R/W logic selection associated with the B access of dual-access units.

Two other functions performed by the IOSELECTED signal are the disabling of the READ ONLY-READ/WRITE switch control on the operator control panel during an I/O operation, and the enabling of the input bus receivers.

Dual-access units require drive selection logic that is a bit more complex, due to interface lockout circuits that prevent simultaneous access. Dual-access control is covered under the following heading.

DUAL-ACCESS CONTROL

The dual-access option is an extension of the standard single-access interface and provides a means by which two controllers may gain access to a single drive on a time-shared basis.

The dual-access option employs the following basic elements:

- Separate line drivers and receivers for each access
- Manual control for each access
- Automatic control logic that prevents simultaneous access selection and allows only one controller to access a common drive at one time
- Fail-safe timers for each access to prevent access hangup in case of a system or component failure

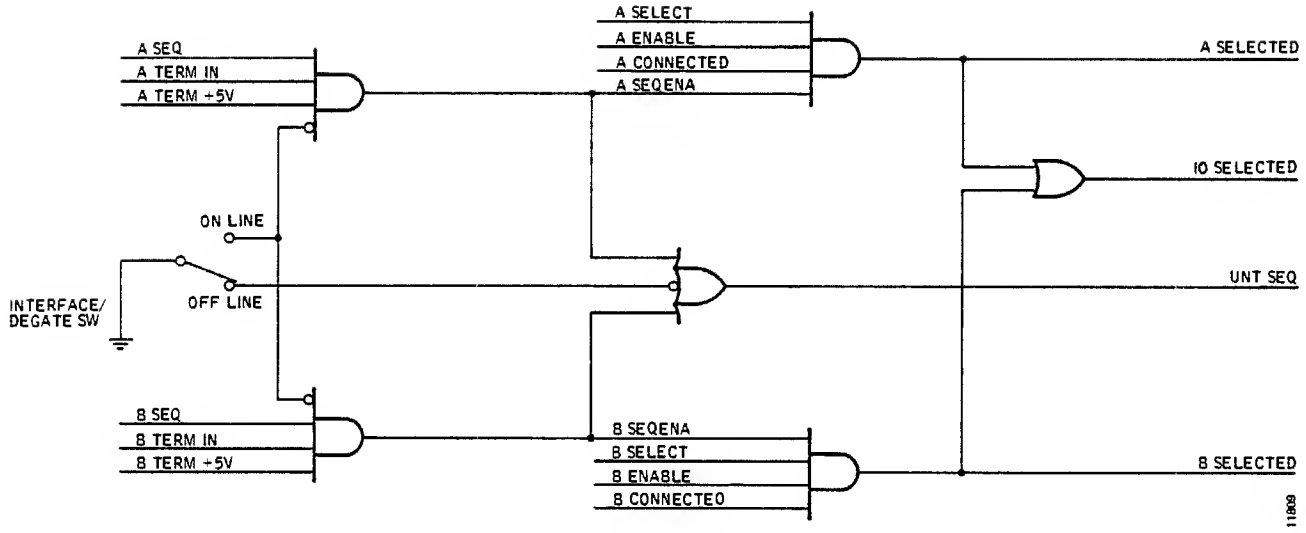

Figure 3-5. Dual Access Drive Selection Logic, Simplified

When two controllers are sharing a disk drive through automatic control, operation is controlled by the controller request signals, the operator-controlled access enable switches, and the automatic control logic. The operator switches override the other controls. Descriptions of the logic involved with the dual-access option are contained in the following paragraphs.

Drive Control Logic

The drive selection logic for dual-access units (Figure 3-5) functions in essentially the same manner as the single-access drive selection logic. The UNTSEQ signal that allows offline power-up or initiates power-down sequencing is developed as in single-access drives. During online operation, the development of UNTSEQ requires that both bused cable terminators be installed (ATERMIN, BTERMIN); otherwise, the dual-access logic that generates UNTSEQ is the same as the single-access logic that performs the same function.

Selecting the drive is necessarily more complex in the dual-access environment because of the interlock signals involved. The select, enable, and connected signals associated with each access must be active for selection of that access. Select signals from the interface are ANDed with enable signals from the manual control logic and connected signals from the auto control logic to produce the selected (A SELECTED, B SELECTED) signals. These signals enable the output line drivers and input receivers, and they return selected status to the controller.

The IO SELECTED signal in dual-access drives performs two functions: it disables the READ ONLY-READ/WRITE switch control on the operator control panel during an I/O operation, and it enables the input bus receivers.

Manual Control Logic

The Dual-Access Manual Control Logic is shown in Figure 3-6. Manual control switches for each access are located on the operator control panel. The configuration of these switches determines the operation of the logic. Table 3-2 shows the switch position states and the corresponding logical operation.

TABLE 3-2. DUAL-ACCESS SWITCH POSITIONS AND OPERATIONS

Access A Switch	Access B Switch	Logical Operation
ON	ON	Automatic
ON	OFF	Manual; forced connection to Access A
OFF	ON	Manual; forced connection to Access B
OFF	OFF	Degated (offline)

Operating under automatic control, both access switches are on and both enable latches are set. When an access is selected, TAG ACTIVE and the respective connected signal (A CONNECTED, B CONNECTED) are both up, thus inhibiting the enable latch from changing and, thereby, preventing an inadvertent termination of an I/O operation.

With both enable latches set, FORCE A and FORCE B are held inactive by the cross-coupling of the complementary latch outputs. When IO ENABLED goes active, AUTO goes active to enable automatic control operation.

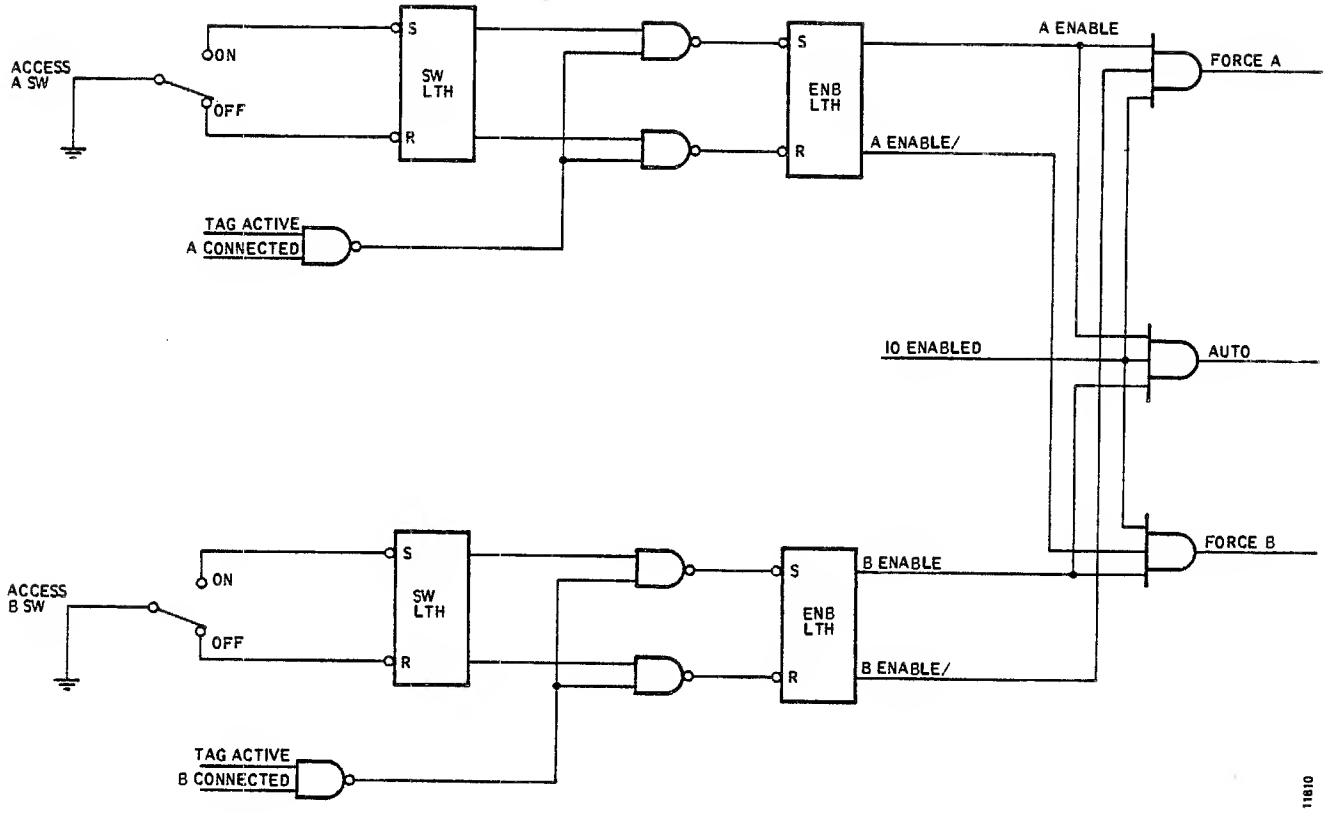

Figure 3-6. Dual Access Manual Control Logic, Simplified

Notice that if the ACCESS B switch is off, FORCE A becomes active when IO ENABLED comes up; the opposite condition is also true. With either switch off, AUTO is held inactive by the enable latch output of the disabled access switch. With both switches off all the output gates are disabled and the drive is degated (offline).

Auto Control Logic

The Dual-Access Auto Control Logic (Figure 3-7) employs a programmable counter (Fail-Safe Timer), Lock-Out Latch, and associated gate logic to control access to the drive for two different controllers. The purpose of this logic is to prevent simultaneous selection by both controllers and to automatically disconnect the access from a reserved controller if no tag line is active within the predetermined time limit of the fail-safe timer.

One timer or the other is normally held in the load mode by the request signal (A REQUEST, B REQUEST) from the opposite access. A request for access by either controller has no effect on the circuit unless the other access is connected (operating) as evidenced by an active A CONNECTED or B CONNECTED signal. As previously mentioned, FORCE A and FORCE B are inactive during automatic operation.

For purposes of illustration, suppose the A access is connected to its controller and B REQUEST goes active. With the tag line (TAG ACTIVE) up, the 400-nanosecond one-shot fires and sets the Fail-Safe Timer in count mode at the end of the output pulse. This starts the timing operation.

The timer begins counting from the preset count value determined by the jumper wire configuration of the Time Select Jumper Socket. This value is variable from 1.3 seconds to 20.8 seconds in 1.3-second increments (clock cycle time). Should TAG ACTIVE drop and then go active again before the timer times out, the one-shot reloads the counter and initiates another count cycle. If TAG ACTIVE drops and remains inactive, the timer times out.

When the timer times out, the A TIMEOUT or B TIMEOUT active signal resets the Lock-Out Latch to allow the requesting controller to capture the drive. The time out signal also loads the Fail-Safe Timer for the next operation.

Dual-Access Operation

The dual-access operation is normally controlled by the interface signals with both access switches left in the ON position. Each radial cable connected to a dual-access drive contains two extra lines. The signals associated with these lines are as follows:

- Request signals generated by each controller — Their purpose is to enable the dual-access control logic so that the drive can be selected.

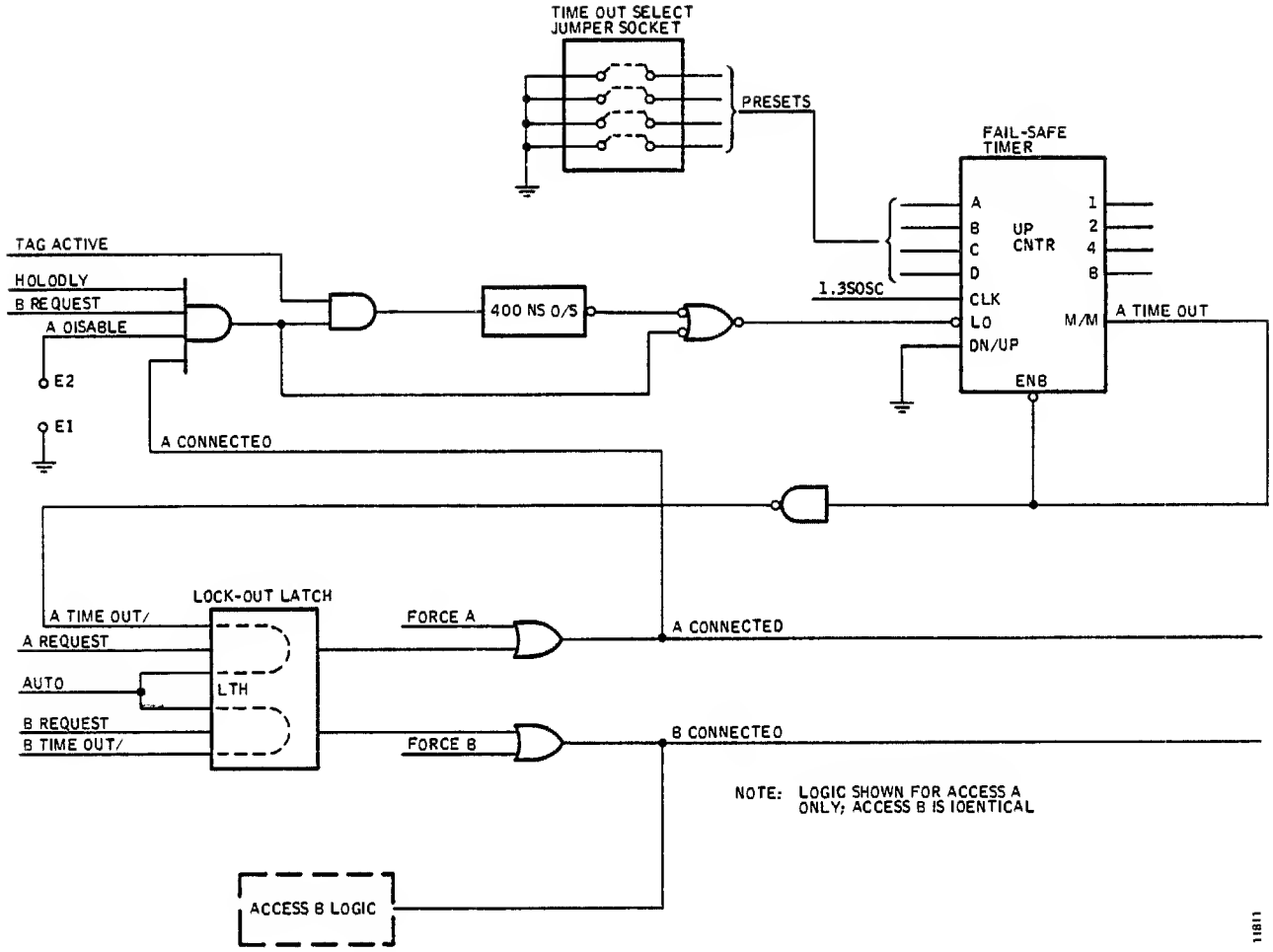

Figure 3-7. Dual Access Auto Control Logic, Simplified

- Request From Other Controller signals generated by the disk drive — Their purpose is to allow systems that require this information to make appropriate decisions in the controller or software

The Request signal from the controller is brought up whenever drive access is desired. If the drive is not connected to the other access, it will be connected to the requesting access. If the drive is connected to the other access, the Request signal triggers the Fail-Safe Timer and it begins timing out. If there is no tag line activity by the using access within the preselected time-out period, the timer times out and enables the requesting access to select the drive.

After the controller is connected to the drive, the Request signal remains active as long as continued use of the drive is required. The tag line must be brought up periodically during the continued use period to ensure that the access remains connected to the drive. Note that the timer only starts when the other access issues a request. When drive access is no longer required, the Request signal is dropped to allow drive usage by the other access. Whenever either access raises its Request signal, the Request From Other Controller is automatically generated by the Status and Error Detection System.

Attention interrupts are generated for the connected controller only. These interrupts are generated in the same manner as for the standard, single-access interface. In addition, an interrupt is generated whenever an access becomes connected, and the interrupt is cleared in the same manner as for single-access units. When the drive is not connected, attention is always reset.

SET CYLINDER CONTROL

Cylinder addresses for head-positioning operations are sent to the drive over the 10 Bus lines along with an active Set Cylinder Tag line signal. The address is presented in binary form, with Bus bit 0 (position 512 in both T200 and T300 drives) being the most-significant bit.

Only cylinder addresses between 000 and 814 are valid. If an address higher than 814 is sent, the disk drive will detect it and set an illegal cylinder address Device Check. Device Check is also set if the heads are offset when the Set Cylinder Tag initiates the seek operation. Either of these types of Device Checks require a Rezero command to reset the Device Check.

With the disk drive selected, an active Set Cylinder Tag line signal causes data on the Bus lines to be loaded into

the drive Cylinder Address Register (CAR). If the address at the outputs of the CAR is legal, dropping the Set Cylinder Tag line signal initiates a seek operation by the Head-Positioning Servo System to the new cylinder address.

A drive-ready Attention is returned to the controller when the seek operation to the new address is completed. If the seek operation is not completed within approximately 0.90 seconds, Seek Incomplete and Attention are set. Attention can be reset by a read command, the start of a seek operation, a rezero operation, or by manually down-sequencing the drive. Seek Incomplete can be reset by manually down-sequencing the drive or by executing a Rezero command.

Figure 3-8 shows the sequence of events for set cylinder control as they occur from drive selection to seek-complete Attention. For sake of clarity, dual access details are omitted in the diagram. The controller may drop the active drive SELECT line signal as soon as the seek operation has started and wait for the Attention signal, or it can continue to monitor the status lines for the drive Ready signal, Device Check, etc.

All operations described can be commanded through the exerciser when the disk drive is offline (DEGATE signal active).

CYLINDER ADDRESS REGISTER (CAR)

The Cylinder Address Register (see Figure 3-9) receives parallel-load inputs from the interface/exerciser multiplexer switches for Bus lines 0 thru 9. Loading is controlled by the SETCYL signal, which is raised when the Set Cylinder Tag line becomes active. The leading edge of SETCYL triggers a 350-nanosecond one-shot to produce a DIFF*S pulse, which strobes the subractor output (difference between the current cylinder address and the new cylinder address on the bus lines) into a Difference Counter in the Head-Positioning Servo System.

When the one-shot times out, a flip-flop called CAR*S is set and causes the new cylinder address on the Bus lines to be loaded into the Cylinder Address Register to replace the cylinder address currently held. CAR*S is reset by the trailing edge of SETCYL, which also initiates the seek operation to the new cylinder address. Cylinder Address Register bits are monitored by gate logic that detects addresses higher than 814 (ILLCYL).

For an illegal cylinder address, ILLCYL goes true in sufficient time to inhibit the start of the seek operation; but since the current cylinder address has been lost and the Difference Counter contains an illegal spurious count, recalibration is necessary. This is why illegal cylinder Device Checks require a Rezero command to reset.

The Cylinder Address Register is reset to zero (cylinder address 000) by load speed control signal LOADSP. This signal from the Head-Positioning Servo System control logic is set when power is turned on, by any head retract operation, including Emergency Retract, and by the Rezero command. CAR reset to cylinder address 000 assumes that the next operation will be a seek operation to that cylinder, making 000 the current cylinder address.

CAR outputs CAR001 thru CAR512 go to the subtractor for difference count determination and to the Illegal Cylinder Detector Logic that checks for a cylinder number greater than 814. CAR001 is used by the Servo Control Logic to determine an odd or even cylinder, and CAR128, CAR256, and CAR512 go to the Read/Write System for write-current zone control.

SET HEAD CONTROL

Addresses for read/write head selection and for offset commands are sent to the drive over seven of the 10 Bus lines along with an active Set Head Tag line signal. The head address is presented on Bus lines 5, 6, 7, 8, and 9 in binary 16, 8, 4, 2, 1 form. Bus line 2 is used to command offset active or offset reset, and Bus line 3 is used to command offset direction; active for forward, inactive for reverse.

With the disk drive selected, an active Set Head Tag line signal causes data on the head address bus lines to be parallel-loaded into the drive Head Address Register (HAR). The outputs of this register are sent directly to the Read/Write System where they are decoded to activate one of 19 lines that select a head for subsequent read or write operations.

The HAR is also a binary up-counter that allows the head address to be advanced or reset under Head Advance and Head Reset (reset to Head 0 address) Control Tag commands. If the head address is greater than 18, the End of Cylinder status signal will be activated.

A flip-flop in the Head-Positioning System stores the offset control command, and the Head Address Register stores the offset direction. Both are activated at the trailing edge of the Set Head Tag signal.

HEAD ADDRESS REGISTER AND OFFSET CONTROL

Figure 3-10 shows the Head Address Register and Offset Control logic in simplified Form. An active Set Head Tag line signal from the controller changes the HAR from count mode to load mode, which loads the HAR with the head address on Bus lines 5, 6, 7, 8, and 9. The outputs of the HAR are monitored at all times by End-of-Cylinder (ENDCYL) detector gates that raise this status signal whenever the head address is greater than 18.

When the Set Head Tag line signal is dropped, the HAR returns to the up-count mode. The head address can subsequently be advanced by one by receiving an HDADV clock. HDADV is provided as a Control Tag command, which will be discussed later.

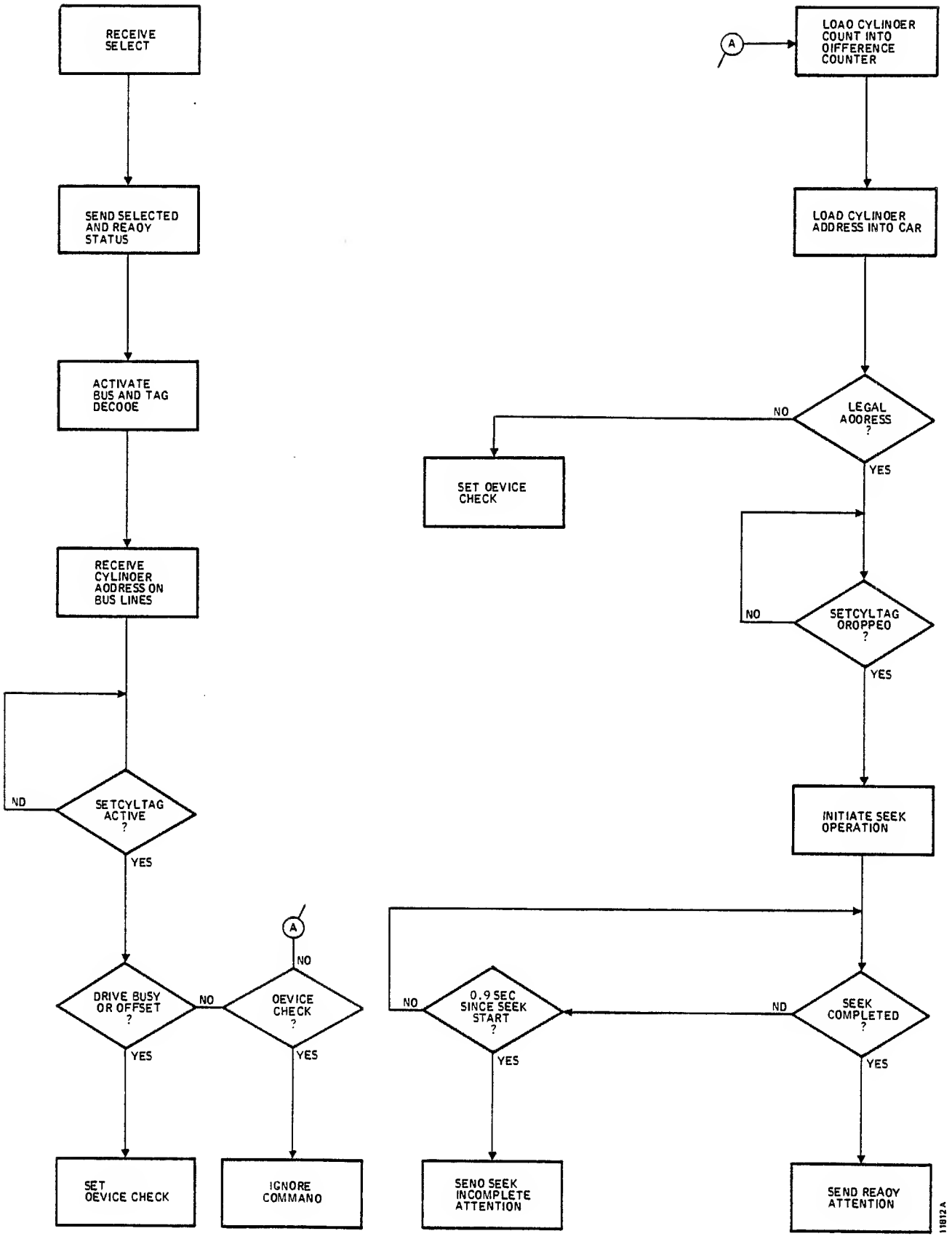

Figure 3-8. Cylinder Address Loading and Seek Start Flow Diagram

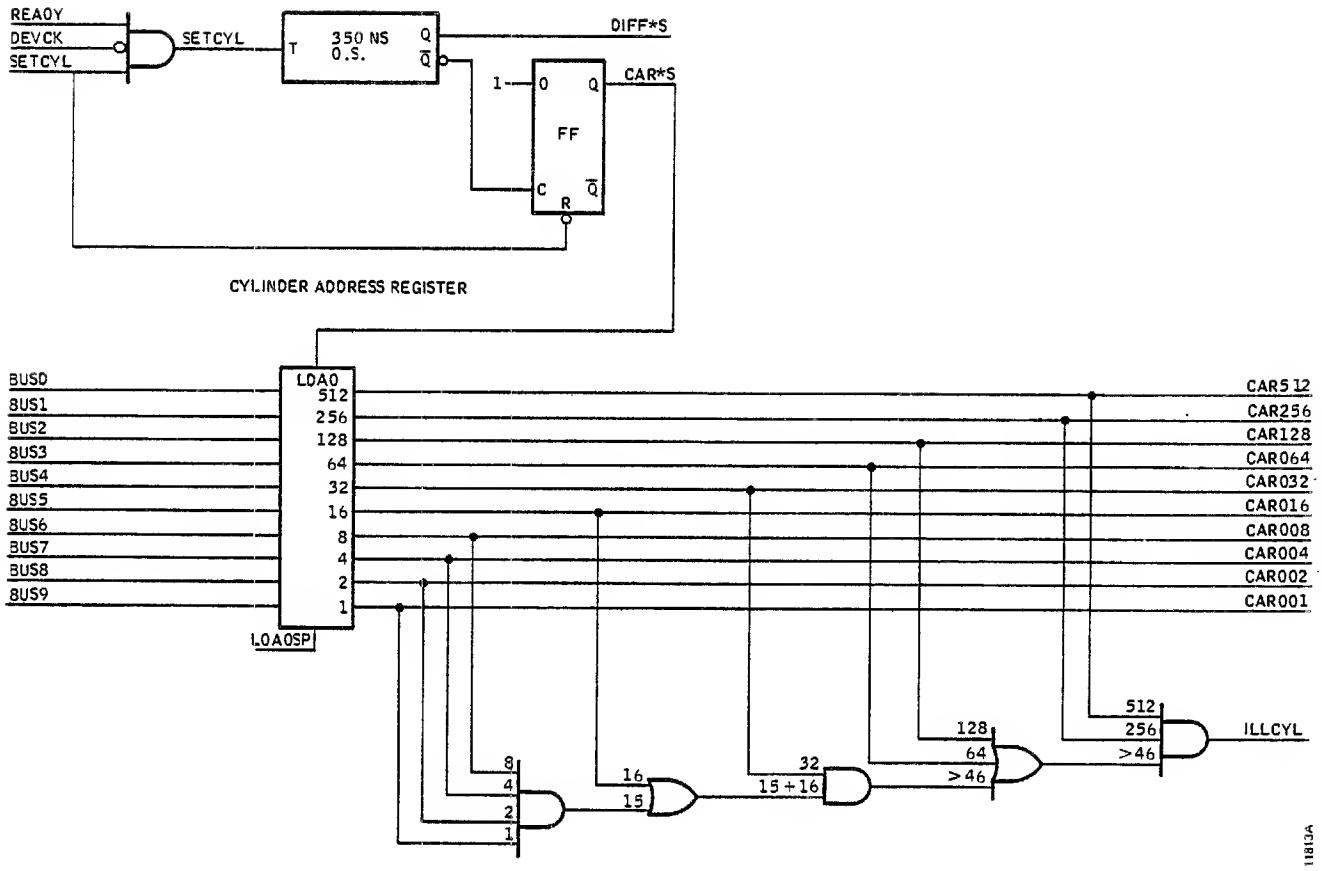

Figure 3-9. Cylinder Address Register Logic, Simplified

If the drive is in the ready condition (heads loaded and no seek operation in progress), READY will be active and the offset flip-flop will be clocked to load the offset command data on Bus line 2 when SETHD drops. Notice that the offset direction information was loaded previously with the head address data. High Bus Line 3 indicates a forward offset direction, and a low on the line sets up a reverse offset direction.

With the offset direction established, a high Bus line 2 sets the offset flip-flop when SETHD falls to initiate an offset operation. If the Bus line is low, no offset is programmed.

The HAR can be reset under either of the following conditions when there is not an emergency retract condition:

- LOADSP active — this occurs during a First Seek or Rezero operation.
- HAR*R active — this is the Reset Heads Control Tag command from the controller

Because of the manner in which the binary head address select lines (HD01-HD08) are developed, one read/write head is always selected on both matrices. This is true whether the Head Select (HDSEL) signal is active or not. The least-significant bit in the HAR (HAR01) qualifies the head selection process to the desired head by gating out the matrix containing the unwanted head. During read operations HAR01 and its complement perform the gating function on the Read Limiter card; during write operations the same signals generate the Write Enable signals (WRENA LM, WRENA RM) show on Figure 3-10. This arrangement ensures that only one of the selected heads is ever active at any given time.

Notice that the gate logic for the right and left matrix address lines is not the same. The left matrix logic always provides active HD01 LM and HD08 LM outputs when HDSEL is inactive. On the left matrix board there is no corresponding active head for that address, so a dummy head is used. Any time an active head is not selected on the left matrix, the dummy head is selected. With HDSEL inactive, all the binary head address select lines for the right matrix are inactive, a condition that automatically selects Head 00.

The Head Unsafe Detection Logic looks for the condition where one head is selected on each matrix. This circiut will be discussed in detail in Section 5.

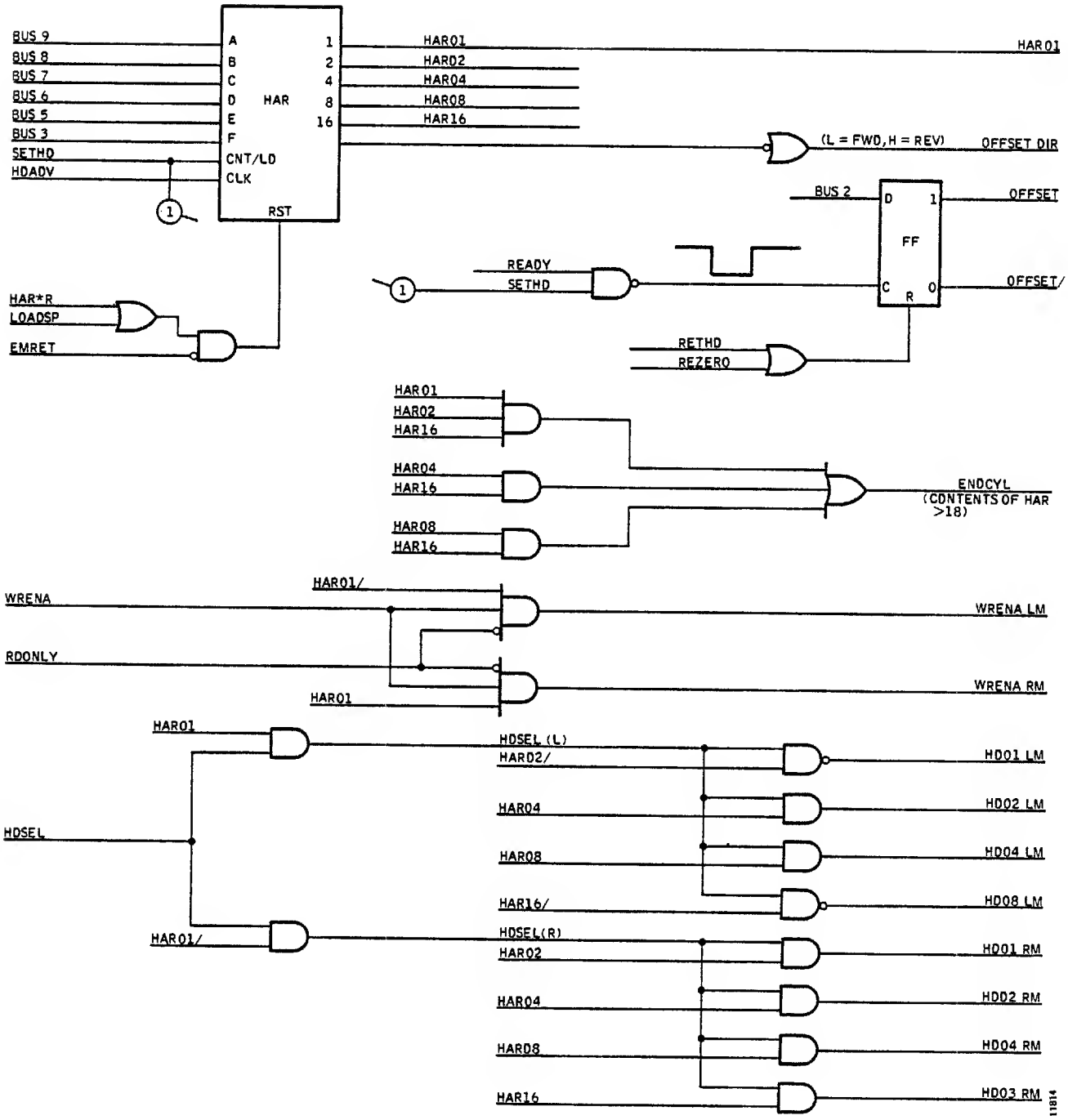

Figure 3-10. Head Address Register and Offset Control Logic, Simplified

CONTROL TAG COMMANDS

All commands other than seek-to-cylinder, set head address, and head offset are detected from the Bus lines when the Control Tag line is active. Control Tag commands include:

- Recalibrate to Cylinder 000 and Head 0 (REZERO)
- Advance to Next Head (HDADV)
- Reset to Head 0 (HAR*R)
- Enable Head Selection (HDSEL)
- Write Data (WRENA)
- Read Data (RDGATE)
- Strobe Read Data Early (STROBE EARLY)
- Strobe Read Data Late (STROBE LATE)
- Enable Address Marks (ADRMK)
- Reset Device Check (DEVCK*R)

The operations performed by these commands are defined more fully in Table 3-3.

TABLE 3-3. CONTROL TAG COMMANDS

Signal	Command Name	Command Function
BUS 0	Strobe Late	Skews read data detection 4 nanoseconds late for attempted read-error recovery.
BUS 1	Strobe Early	Skews read data detection 4 nanoseconds early for attempted read-error recovery.
BUS 2	Write	Turns on circuits to write data.
BUS 3	Read	Turns on read curcuits and resets Attention interrupts.
BUS 4	Address Mark	Commands an address mark to be generated, if writing; or enables the address mark detector, if reading.
BUS 5	Reset Head Register	Resets HAR to Head Address 0.
BUS 6	Device Check Reset	Resets most types of Device Check errors unless an error condition is still present.
BUS 7	Head Select	Turns on the head-selection circuits. Head Select must be active 5 or 15 microseconds before Write or Read is commanded, respectively.
BUS 8	Rezero	Repositions the heads to cylinder 000, selects Head Address 0, and resets some types of Device Checks.
BUS 9	Head Advance	Increases Head Address count by one.

If the disk drive is selected, online, and Device Check is not set when the Control Tag line becomes active, Bus lines 0, 1, 2, 3, 4, 5, 7, and 9 will be gated to the other disk drive systems as control commands. See logic diagram, Figure 3-11. Normally, such operations as read/write, head select, and head advance are sequenced by the controller raising and dropping and appropriate Bus line signals while keeping the Control Tag line active.

That is to say, the majority of Control Tag commands are unbuffered, level-type commands that will be responded to as long as they are high.

Device Check Reset and Rezero commands will be executed regardless of the status of Device Check. This is so because both are commands used to reset a Device Check. DEVCK*R is a direct-reset signal for most Device Check errors. REZERO resets Device Checks due to seek-while-offset or seek-to-illegal-cylinder commands and also initiates a Rezero operation by the Head-Positioning Servo System. The flip-flop that generates REZERO is set directly by the rising edge of the Control Tag line signal if the Bus 8 line is active. The reset signal for REZERO is LOADSP (load speed), which is turned

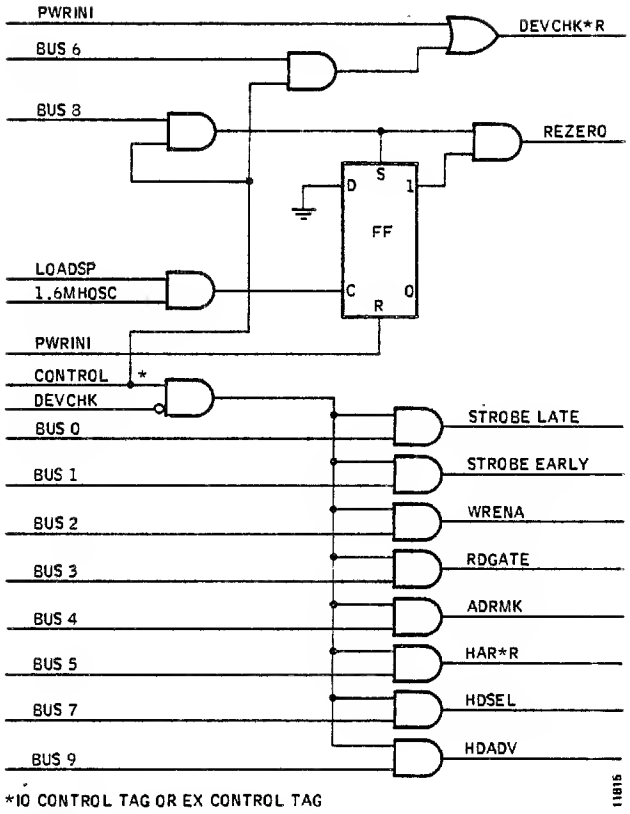

Figure 3-11. Control Tag Command Decode Logic, Simplified

on by the Head-Positioning Servo System in response to the Rezero command. Initial reset is a function of the PWRINI pulse.

INDEX DETECTION

The starting point of each cylinder is marked on the servo head surface by a sequence of three missing dibit transitions, providing an index marker once per revolution of the pack. This index marker is used as a reference point by the controller in the location-addressing of records stored on or retrieved from the pack.

The index marker shows up in the dibit signal read from the servo surface as a space-mark-space-mark-mark-space pattern. A pulsed dibit signal, called GAPCLK, from the Head-Positioning Servo System is monitored by an Index Detector that consists primarily of two one-shot multivibrators and five flip-flops. See Figure 3-12. Each time the pattern of missing dibit just described is detected in the GAPCLK signal, a 4-microsecond index pulse, INDEX, is produced by the detector. INDEX is sent back to the controller as status.

A timing diagram, Figure 3-13 shows how the Index Detector works. The rising edge of the 403KHZOSC clock triggers a 100-nanosecond Reset one-shot, which produces repetitive, short reset pulses for the first flip-flop, called FFA for purposes of discussion. This flip-flop is clock-set by the rising edge of each GAPCLK/

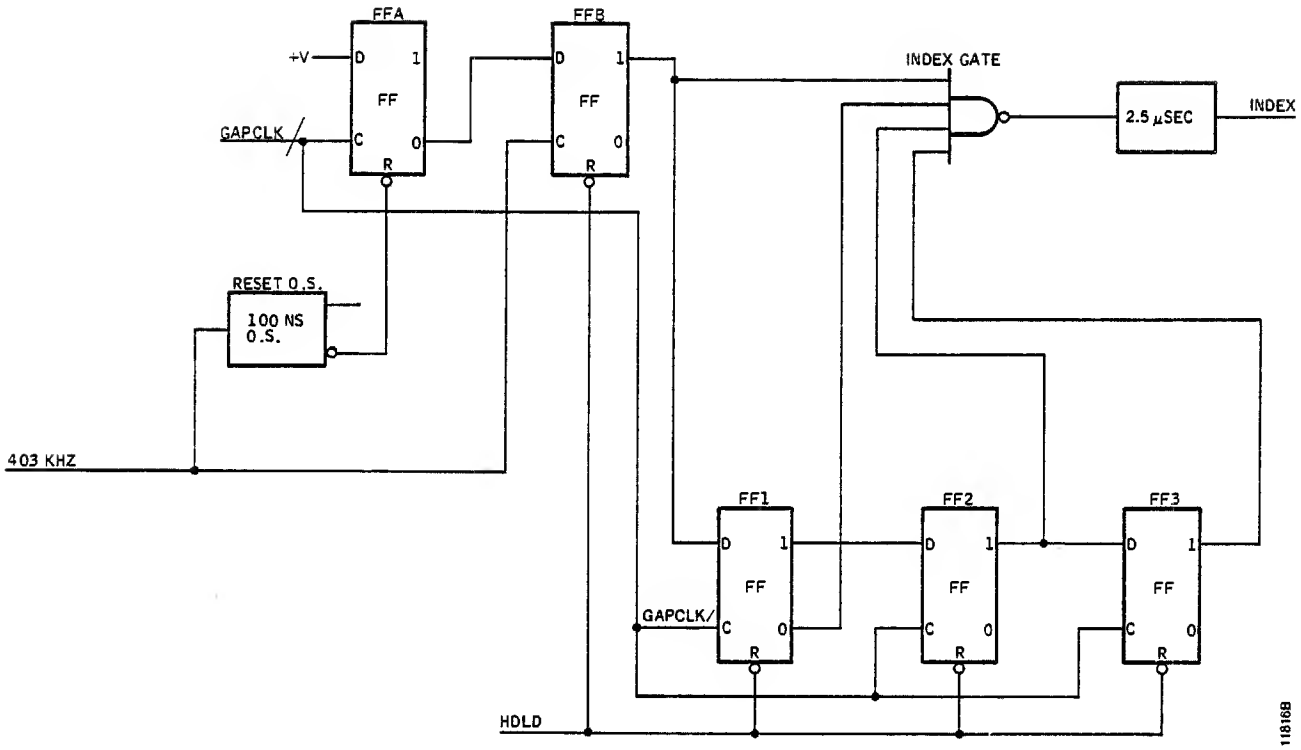

Figure 3-12. Index Detector Logic, Simplified

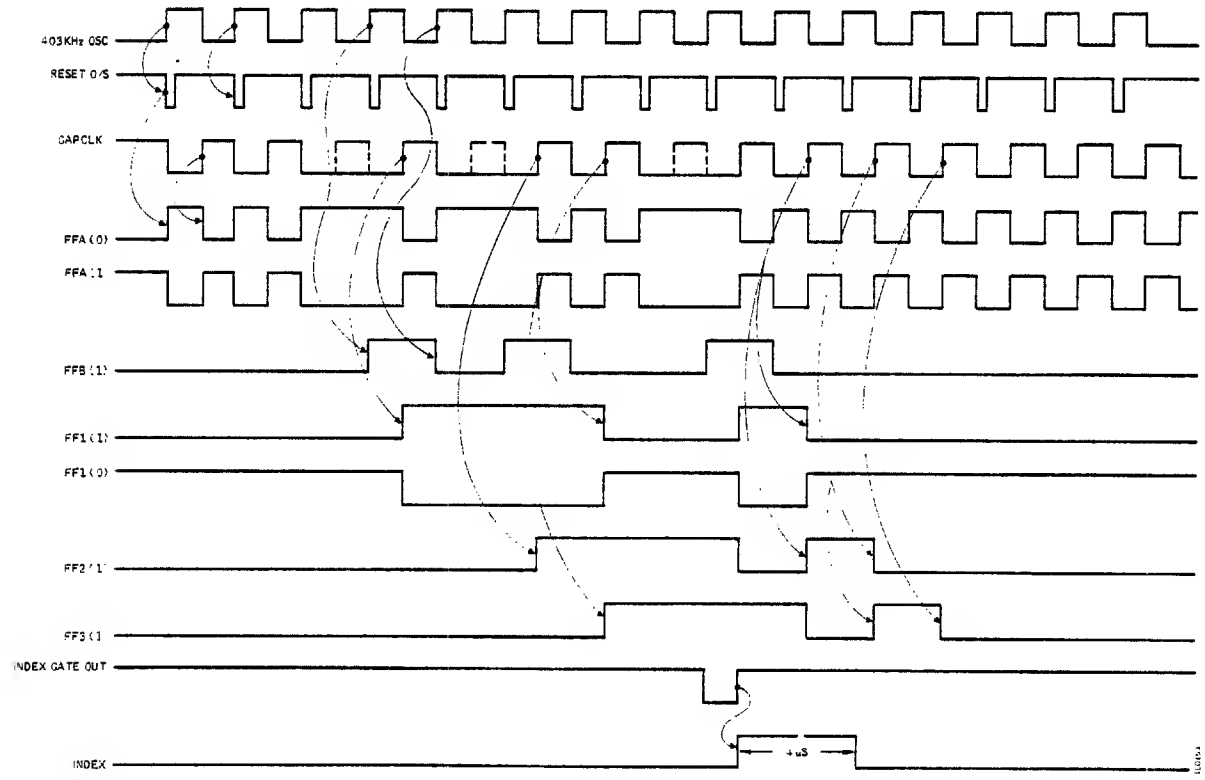

Figure 3-13. Gapclock Index Detection Timing Diagram

pulse and subsequently reset by the Reset one-shot output pulse. Notice that the next flip-flop in line, FFB, is clocked by the rising edges of the 403KHZOSC clock, but canot be set if FFA is set (or HDLD is low, which will be explained in a moment).

Flip-Flop FFB will be clock-set only if a missing dibit pulse fails to set FFA. The rising edge of the next GAPCLK/ pulse clocks FFA and FF1 set and causes FFB to be reset by the rising edge of the next 403KHZOSC clock. The second missing dibit pulse permits FFB to be set again, which keeps FF1 set when the next GAPCLK/ pulse comes along. Flip-flop FF2 is set at this time, which enables FF3 to be set by the next GAPCLK/ pulse.

The third missing GAPCLK/ pulse sets up conditions for setting FFB, which satisfies all conditions of the Index Gate. The output of the Index Gate goes low when FFB·FF1/·FF2·FF3 is true. It rises again when the next GAPCLK/ pulse sets FF1 and resets FF2. A 4-microsecond one-shot is triggered by the rising edge of the gate output to produce the high index output pulse. A low HDLD signal (heads are not loaded) inhibits the detector flip-flops. Because of the asymetrical pattern of missing dibits in the index marker, the flip-flop configuration that satisfies the index gate requirements will not occur if the disk pack is turning backwards, or if random dibit dropout occurs.

SECTOR COUNTER

The fixed-length sectoring function employs a 12-bit down-counter whose side-load starting count is jumper-wire programmable for bytes-per-sector selection. See Figure 3-14. Jumpers are installed for zeros in the positional notation of the binary bytes-per-sector number. This number is side loaded into the counter by a 350-nanosecond one-shot that is triggered by the leading edge of each Index and Sector pulse.

The intitial side-load count is counted down to zero (MIN output high) by the 806KHZ clock. When the MIN count is reached, the trailing edge of the same clock pulse sets the SECTOR flip-flop, triggering the one-shot to reload the counter, which drops the MIN output. One clock interval (1.24 microseconds) later, the SECTOR flip-flop is clocked reset.

The SECTOR flip-flop is inhibited from generating an output by a second flip-flop that is held reset whenever LOADSP is high. Consequently, SECTOR pulses are not produced during drive not-ready head load and head unload intervals. The first index pulse after head loading is complete (LOADSP goes low) sets the enabling flip-flop and loads the counter. Each subsequent index pulse resynchronizes the sectoring function by a counter load operation.

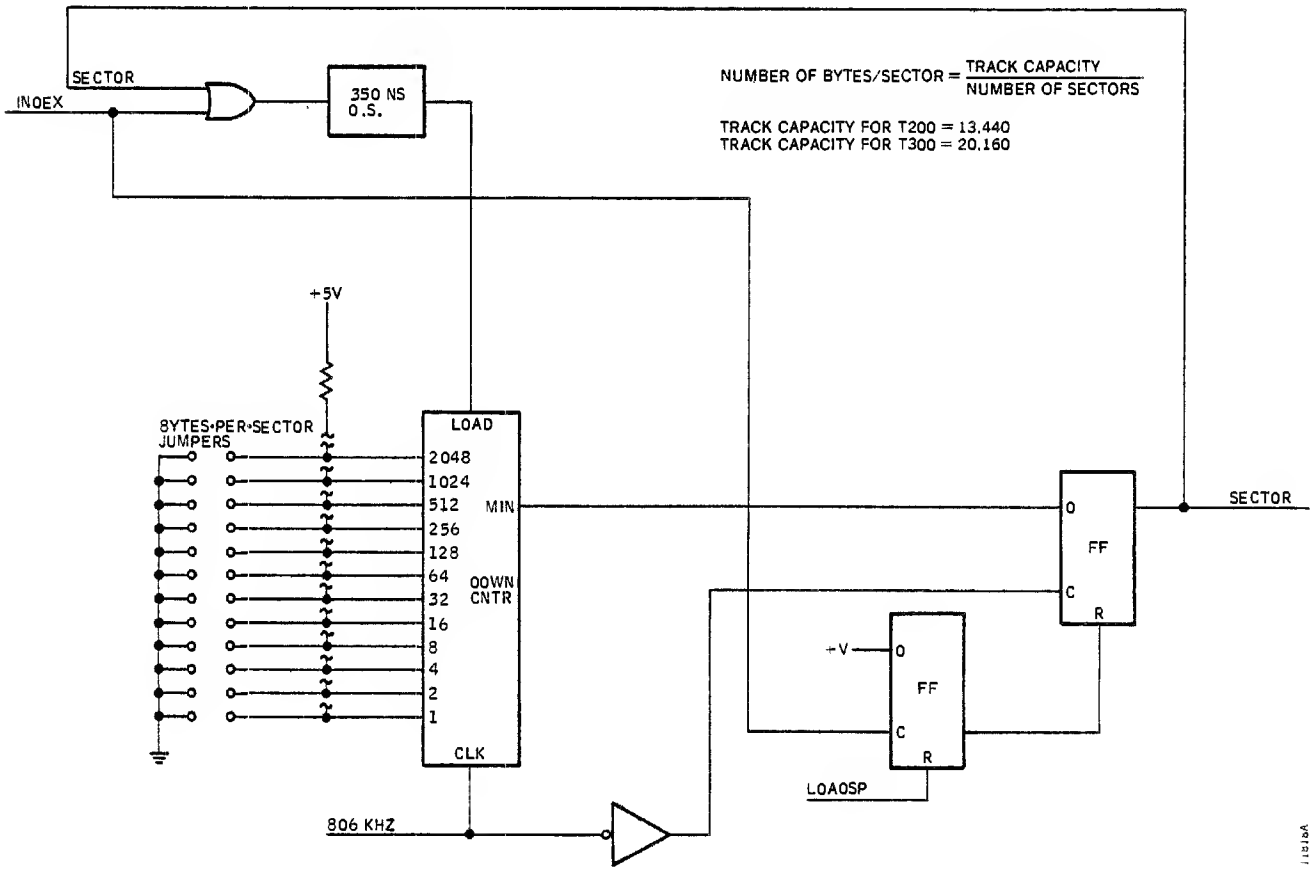

Figure 3-14. Fixed-Length Sector Counter, Simplified

Since the T300 disk drive has a 50 percent greater bit packing density than the T200 drive (6060 bpi as opposed to 4040 bpi), the interval between 806KHZ clock pulses represents a one-and-one-half byte time interval in T300 machines. Because of this difference, the number of bytes per sector desired must be divided by 1.5 to arrive at the effective side-load count when jumper-programming the Sector Counter in any T300 drive. True maximum sector length for these drives is 6144 (1.5 times the 4096 modules of the counter).

SECTION 4
HEAD-POSITIONING SERVO SYSTEM

This system contains the linear motor and all its control circuits. The functions performed by this system include actual head loading and unloading sequence, positioning the heads at cylinder addressed (seek operations), and track following under servo head control.

Figure 4-1 shows the primary components of this system. They include:

- Servo Control Logic
- Subtractor
- Difference Counter
- Digital/Analog Converter
- Servo Amplifier
- Phase Splitter
- Average Detector
- Dibit Filter
- Servo Phase-Locked Oscillator
- Position Error Detector
- Heads-Loaded Detector
- Clock Divider Logic
- Upper Threshold Detector
- Difference Clock Generator
- Velocity/Offset Amplifier
- Track Follow Amplifier
- Drive Amplifier
- Linear Motor with Velocity Tachometer

The Servo Control Logic receives head-positioning commands from the Interface and Control System and Disk Pack System and translates them into execution sequences of control signals. It is this logic section that switches from velocity to track-following modes of operation and controls speed and direction.

A subtractor monitors the bus lines and the output of the Cylinder Address Register, producing a cylinder value of the difference between the two numbers. This value is valid only when a new cylinder address is on the bus lines and the Set Cylinder Tag line is active. At that time, the cylinder difference value is loaded into the Difference Counter and the sign of the difference value is used to set a flip-flop that controls forward or reverse direction of carriage movement. If the sign is positive, the carriage is moved in the forward direction.

The difference count is changed to an analog voltage that is directly proportional to its count value by a monitoring D/A Converter. This converter also produces set analog voltages appropriate to the fixed values for load speed with heads loaded or unloaded. Note that this analog voltage is significant only in magnitude. A forward/reverse switch, controlled by the Servo Control forward/reverse flip-flop, determines the polarity of the analog voltage and thereby determines the direction the carriage will be moved by the linear motor.

The drive amplifier for the linear motor is turned on and off by a Servo Enable signal from the Servo Control Logic. The summing junction at the input to this amplifier receives a velocity control voltage from a Velocity amplifier during seek mode operation. This voltage is the algebraic sum of the analog voltage from the forward/reverse switch and the bucking feedback produced by the velocity tachometer on the linear motor. In track-following mode, the drive amplifier summing junction receives the error signal developed by the servo head Position Error Detector, the velocity tachometer signal, and a plus or minus command offset voltage, if any. When an offset operation is programmed by the controller in an attempt to recover data, an offset amplifier feeds a predetermined voltage to the summing junction through a switch activated by the offset line. Voltage polarity is determined by the controller via the Interface and Control System.

The servo head and its preamplifier are operationally part of this system. The servo preamp signal is amplified by the servo amplifier, and then sent to a switching circuit called the Phase Splitter. The function of the Phase Splitter is to make sure that the polarity of the position error signal, produced during track following, will drive the heads toward the null point of cylinder center. It does this by monitoring the least-significant bit of the current address in the Cylinder Address Register (odd or even indicator) and inverting the servo head signal if the cylinder address is even.

The output of the Phase Splitter goes to the Interface and Control System Index Detector, to the Servo Phase-Locked Oscillator, and to an Average Detector. The Average Detector samples the Phase Splitter servo signal to determine the amplitudes of the plus and minus components of the signal. The pulses from the detector are detected by a Heads-Loaded circuit that provides the Servo Control logic with an indication

that a servo signal is present (heads are loaded). Heads loaded is also sent to the Status and Error Detection system as a status indication that the disk drive is online.

The Position Error Detector processes detector output pulses into a position error voltage that is fed to the drive amplifier summing junction during the track-following mode. The Position signal is zero volt when the servo head is on track center and swings positive or negative as much as 2 volts between tracks.

An upper threshold Detector circuit monitors the Position signal and is triggered by a ±0.75-volt signal amplitude, indicating that the servo head is greater than 500 microinches off track center. Upper threshold drops out at ±0.20 volt when the servo head is closer than 130 microinches to track center. Upper threshold is used by the Servo Control logic to switch from velocity mode to track-following mode. It also provides track-crossing pulses during seek operations from which the clocks are developed to count down the Difference Counter.

The Servo Phase-Locked Oscillator generates clock pulses at 19.2 megahertz. The oscillator output is phase locked to the servo signal by dividing the oscillator output down to 403 kHz and feeding it back to the Dibit Filter that controls the oscillator. That circuit provides a balanced, symmetrical dibit signal regardless of servo head position; this arrangement provides for better oscillator stability and detection of the missing dibits (GAP CLOCK) in the index area.

The Clock Divider Logic divides the oscillator output down to the PLO bit rate frequency used in write data timing and other frequencies used for general disk drive timing.

SERVO CONTROL LOGIC

The servo control logic programs the operation to be performed by the servo system. These operations include:

- Initial head loading (first seek)
- Track-following (detent on cylinder)
- Program seek (seek to selected cylinder)
- Recalibrate (rezero disk drive)
- Head retract (normal head unloading)

To help explain the servo control logic. association of the elements involved in each operation noted above will be described. During the following discussions, initialization of the subject logic will be assumed. Refer to Figure 4-2 during the ensuing discussions.

There are several general comments that should be considered before going into the details of the servo control logic.

- The direction flip-flop (FWD FF) is directly set during a first seek or rezero operation and clock-set during a program seek. Also notice that the reset signal for both the FWD and ODD flip-flops is common.

- The LOADSP flip-flop controls head carriage velocity and generates VELENA during first seek and rezero operations, while the SKENA flip-flop performs the same function during program seek operations. LOADSP commands a set velocity, and SKENA commands a variable velocity according to the length of the seek.

- The ODD flip-flop functions during first seek, rezero, and program seek operations. This signal determines the correct phasing for detent operations.

First-Seek Operation

At the completion of the power-up sequence, the Heads-extended latch (HDEXTLTH) signal is inactive because the heads are retracted; HDEXTLTH/ is therefore high at the D input of the First Seek (FS) flip-flop. When the sequence counter in the power-sequencing system counts out, the Retract Heads (RETHD) signal falls (see Figure 4-3) and clocks the FS flip-flop on. FS directly sets the Forward (FWD) flip-flop, and FS/ generates Servo Enable (SRVOENA). The head carriage must move immediately because FS is ANDed with a 328-millisecond oscillator, and the FS flip-flop is reset at the end of the clock cycle time. As soon as the head carriage moves, HDEXTLTH/ becomes active and holds SRVOENA up so that the operation may proceed. Notice that the Load Speed (LOADSP) flip-flop is set by an active RETHD signal and is thereby conditioned for the first seek operation before it commences. Velocity Enable (VELENA) is also active before the start of this operation, since it tracks LOADSP.

The head carriage drives forward under the influence of LOADSP until the servo head begins picking up recorded tracks on the outer guard band. Heads-Loaded (HDLD) then goes high, followed by Heads-Loaded Delay (HDLDDLY) approximately 3.5 milliseconds later. HDLDDLY sets the TRKFL flip-flop, and TRKFL in turn resets the LOADSP flip-flop, causing VELENA to fall. These conditions put the servo system in the track-following mode with servo speed and direction under control of the POSITION signal. With the Servo head in the outer guard band, the POSITION signal is a steady minus 2 volts due to the absence of any minus-pattern signal. This voltage continues to drive the carriage and heads forward, but at reduced speed.

The servo system will automatically home in on Cylinder 000, because this is where the first Position null point occurs (first time a true dibit signal will be detected). If the carriage and heads overshoot the

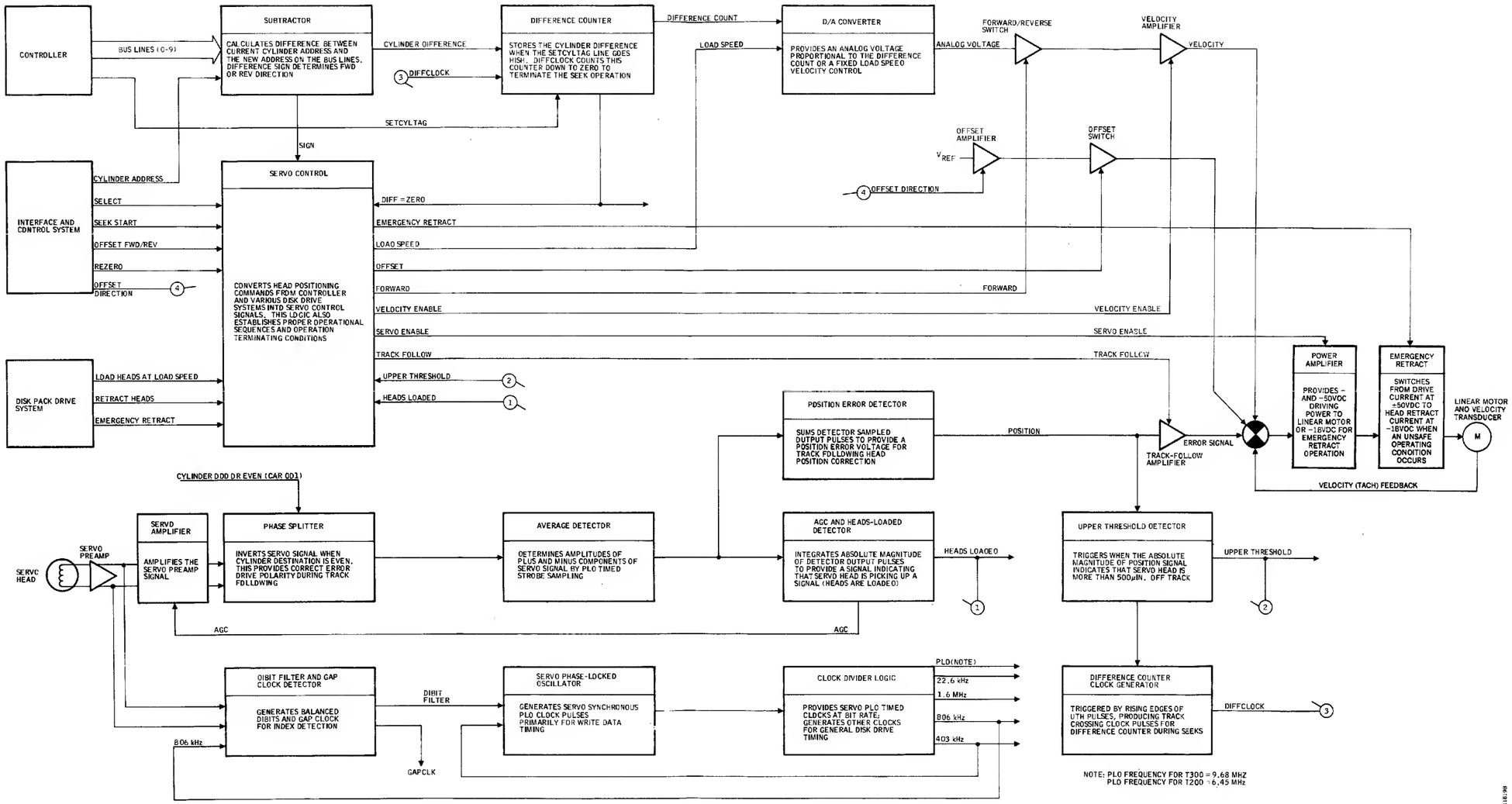

Figure 4-1. Head Positioning Servo System, Block Diagram

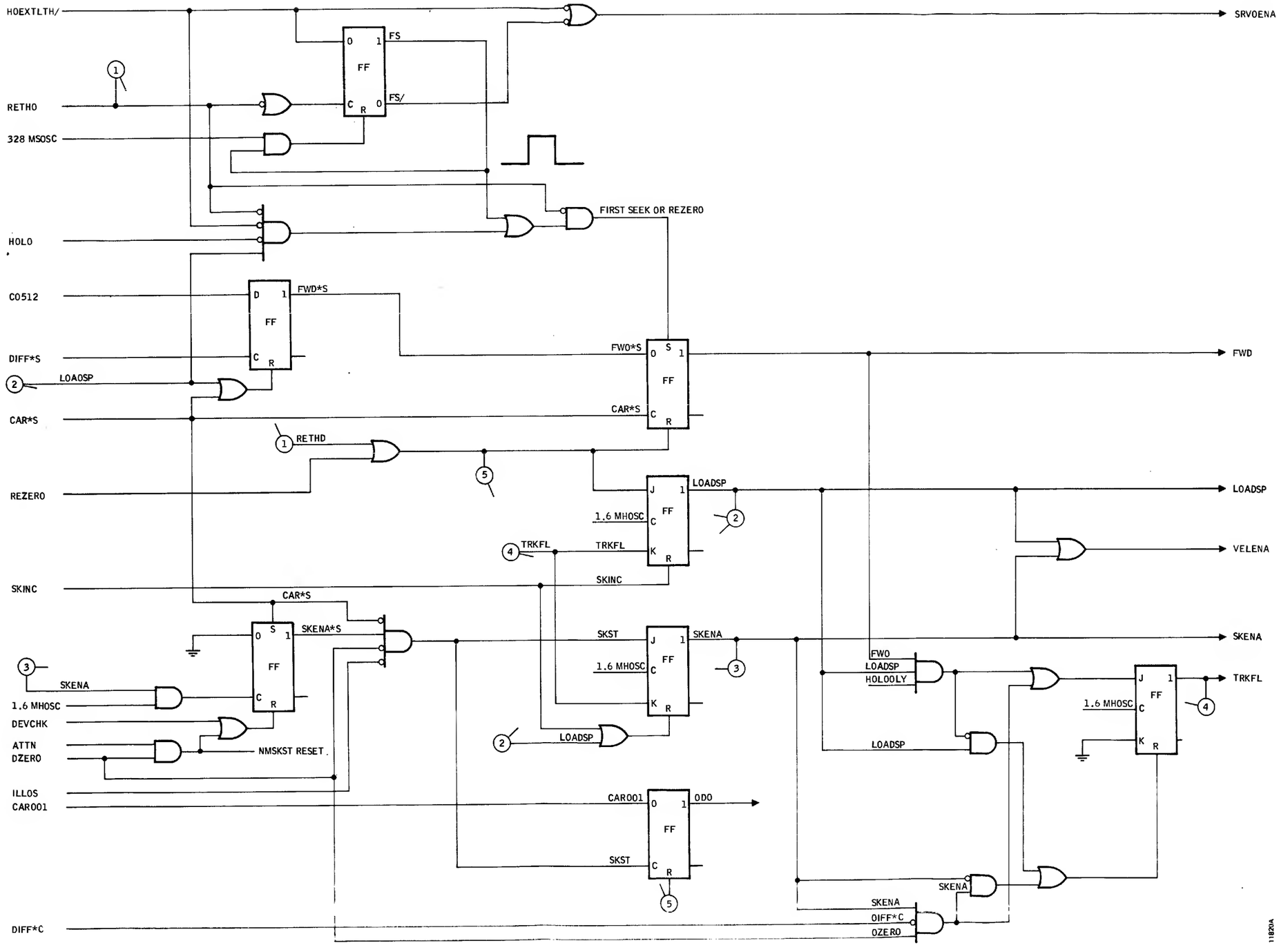

Figure 4-2. Servo Control Logic, Simplified

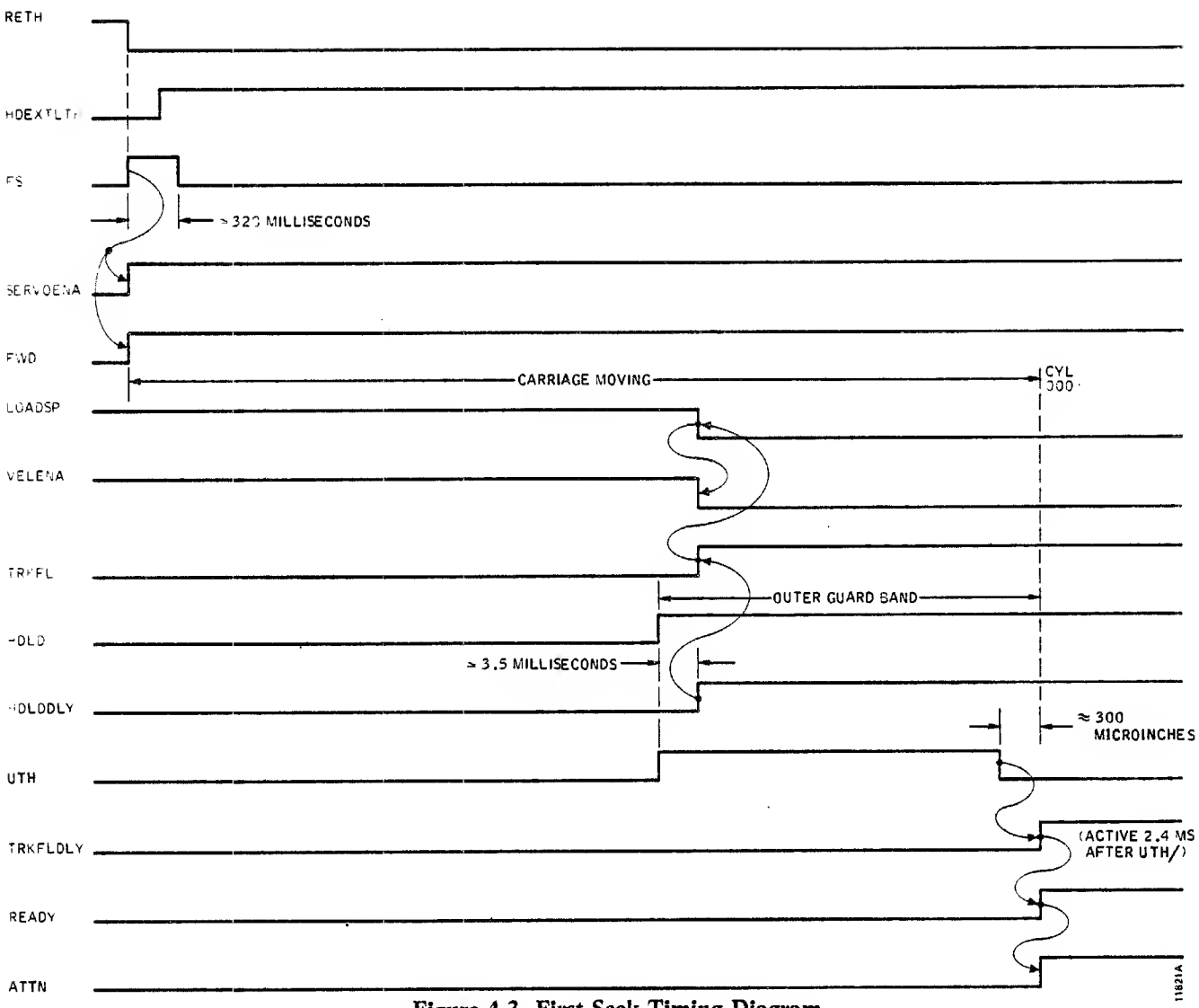

Figure 4-3. First Seek Timing Diagram

cylinder, the POSITION signal will cross the null point and will reverse its polarity, causing the carriage to be driven in the reverse direction back to track center of Cylinder 000. As the Servo head approaches Cylinder 000, the POSITION signal drops and UTH drops out, which allows a 2.4-millisecond count time (TRKFLDLY) to begin. After the delay, drive ready (READY) and Attention (ATTN) are set.

Programmed-Seek Operation

Programmed-seek operations are initiated after the controller has selected the drive and received the selected status return signal. See Figure 4-4. The Bus lines must carry the new cylinder address at least 200 nanoseconds before the controller brings up the Set Cylinder Tag line. This timing constraint allows the subtractor to calculate a valid difference count and to propagate a carry-out that determines the seek direction.

Raising SET CYL triggers the Difference Set (DIFF*S) one-shot on for 350 nanoseconds, (see Figure 3-9 for DIFF*S logic) activating the difference counter load inputs. The 350 nanoseconds during which DIFF*S is active allows the Subtractor Outputs to settle out after a FWD*S carry-in is applied. Refer to the discussion involving the Subtractor and Difference Counter for clarification of this last point. DIFF*S clocks the carry-out signal (C0S12) from the Subtractor into the Forward Set (FWD'S) flip-flop: this signal determines the seek direction.

When DIFF*S drops, the load inputs to the Difference Counter are disabled, the seek direction is locked in the FWD*S flip-flop, and CAR*S is raised to load the new cylinder address on the Bus lines into the CAR to replace the old address. CAR*S also clocks the seek direction into the FWD flip-flop, resets the FWD*S flip-flop, and directly sets the Seek Enable Set (SKENA*S) flip-flop. Nothing further happens until the controller drops the SETCYL tag line.

When SETCYL falls, the CAR*S flip-flop is reset, and the Seek Start (SKST) signal in the Servo Control Logic goes active unless there is a zero loaded into the Difference Counter or an illegal cylinder address in the CAR. The former condition is not necessarily an

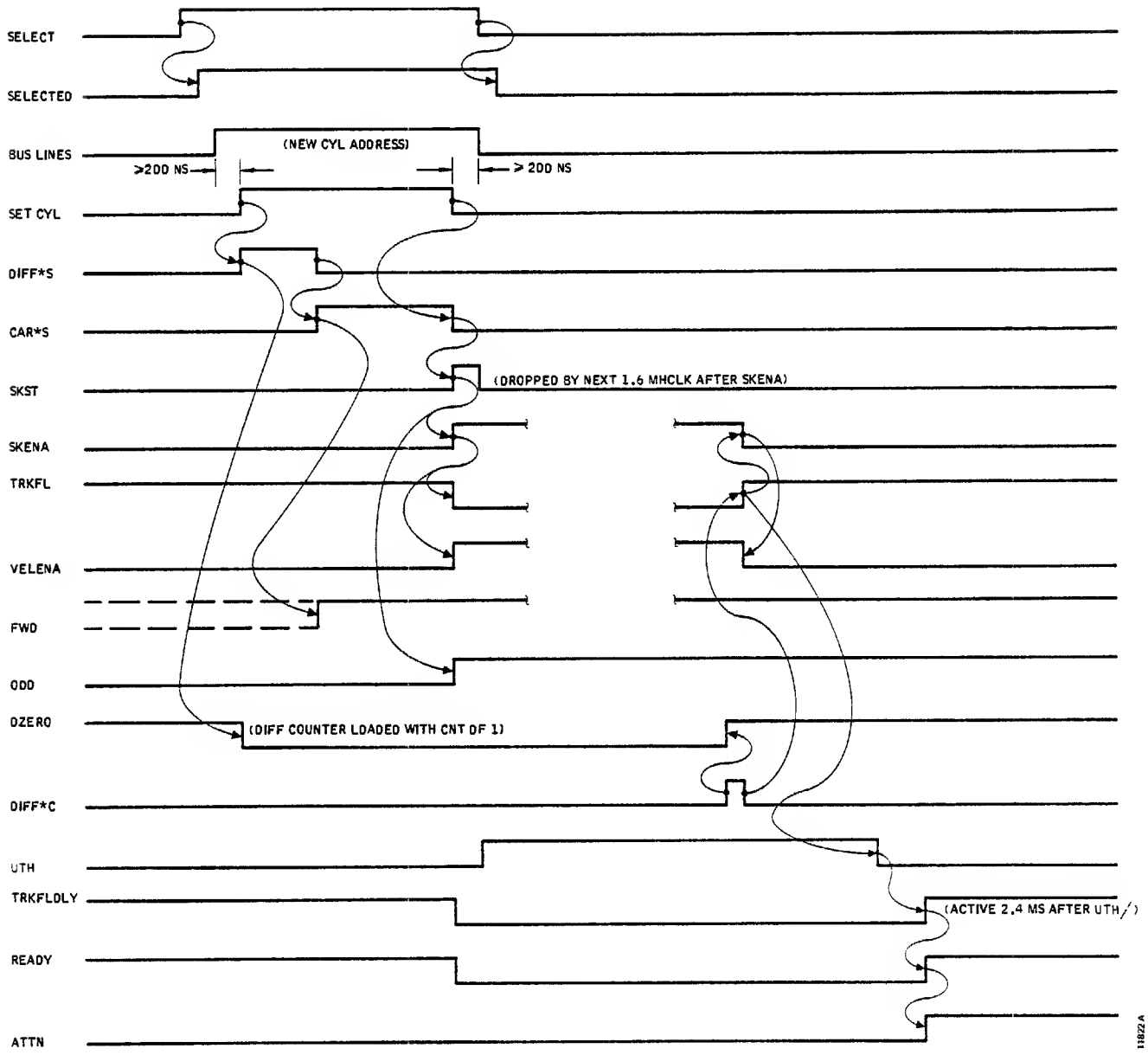

Figure 4-4. Program Seek Timing Diagram (Cy1000 to Cy1001)

error condition and will be explained shortly. The Bus lines must also remain valid for 200 nanoseconds after SETCYL falls.

The SKST signal is active for one clock time and it brings up Seek Enable (SKENA) and clocks the even or odd number residing in the least-significant bit of the CAR (CAR001) into the ODD flip-flop. The example shown indicates that the ODD signal is active, since the seek is to an odd-numbered cylinder.

When SKENA comes up, it causes the TRKFL flip-flop to reset, and it generates VELENA. These events release the servo system from its detented position and enable it to move toward the selected cylinder.

The DIFF*C generated by the last cylinder crossing before the carriage reaches the chosen cylinder brings DZERO up, indicating that the upcoming cylinder is truly the selected cylinder. As the carriage coasts toward this cylinder, DIFF*C falls, and this event sets the TRKFL flip-flop. TRKFL drops SKENA, which in turn drops VELENA, and the POSITION signal assumes control of the head carriage. Approximately 2.4 milliseconds later, TRKFLDLY goes active; this brings up READY, which then brings up ATTN.

For purposes of software expediency, some controllers generate No Motion Seek Start (NMSKST) commands. What this actually means is that the controller sends the required motion commands but does not

send a new cylinder address, so the difference counter retains a count of zero. When this happens in Trident T200 and T300 disk drives, the ATTN latch in the Error Detection and Status System is directly set. With ATTN and DZERO both active, the SKENA*S flip-flop is reset to inhibit SKST, and the ATTN signal remains up to notify the controller that the drive is waiting for the next command.

Rezero Operation

A rezero operation is initiated whenever the Rezero flip-flop in the Interface and Control logic (see Figure 3-10) is set by a rezero command. The servo control sequence initiated by this command is shown in Figure 4-5.

During a rezero operation, the rezero pulse directly resets the FWD and ODD flip-flops and sets the LOADSP flip-flop on the clock. LOADSP brings up VELENA and drops REZERO on the clock. With LOADSP high and FWD low, one of the reset gates to the TRKFL flip-flop is enabled. When TRKFL drops, the head carriage begins moving in reverse.

When the carriage drives out of the outer guard band, the servo head loses the prerecorded dibit pattern and HDLD falls. This event directly sets the FWD flip-flop, causing the head carriage to stop and reverse its direction to forward drive. As the carriage drives back into the disk pack, the servo head again picks up the dibit pattern and HDLD becomes active. With HDLD active, HDLDDLY becomes active approximately 3.5 milliseconds later, and one of the set gates to the TRKFL flip-flop is made, causing TRKFL to become active.

TRKFL resets the LOADSP flip-flop, VELENA falls, and the head carriage is driven into cylinder 000 by the track-following POSITION signal.

Head-Retract Operation

A head-retract operation may be either scheduled or unscheduled (i.e., an emergency retraction); the operation of the servo control logic is the same in either case.

The heads are retracted as the first operation executed in a power-down sequence. Power-Sequencing logic raises the RETHD signal as a result of the START/STOP switch being set to STOP or because the controller drops the active SEQUENCE line. Figure 4-6 shows the sequence of events that occur thereafter for head-retract control.

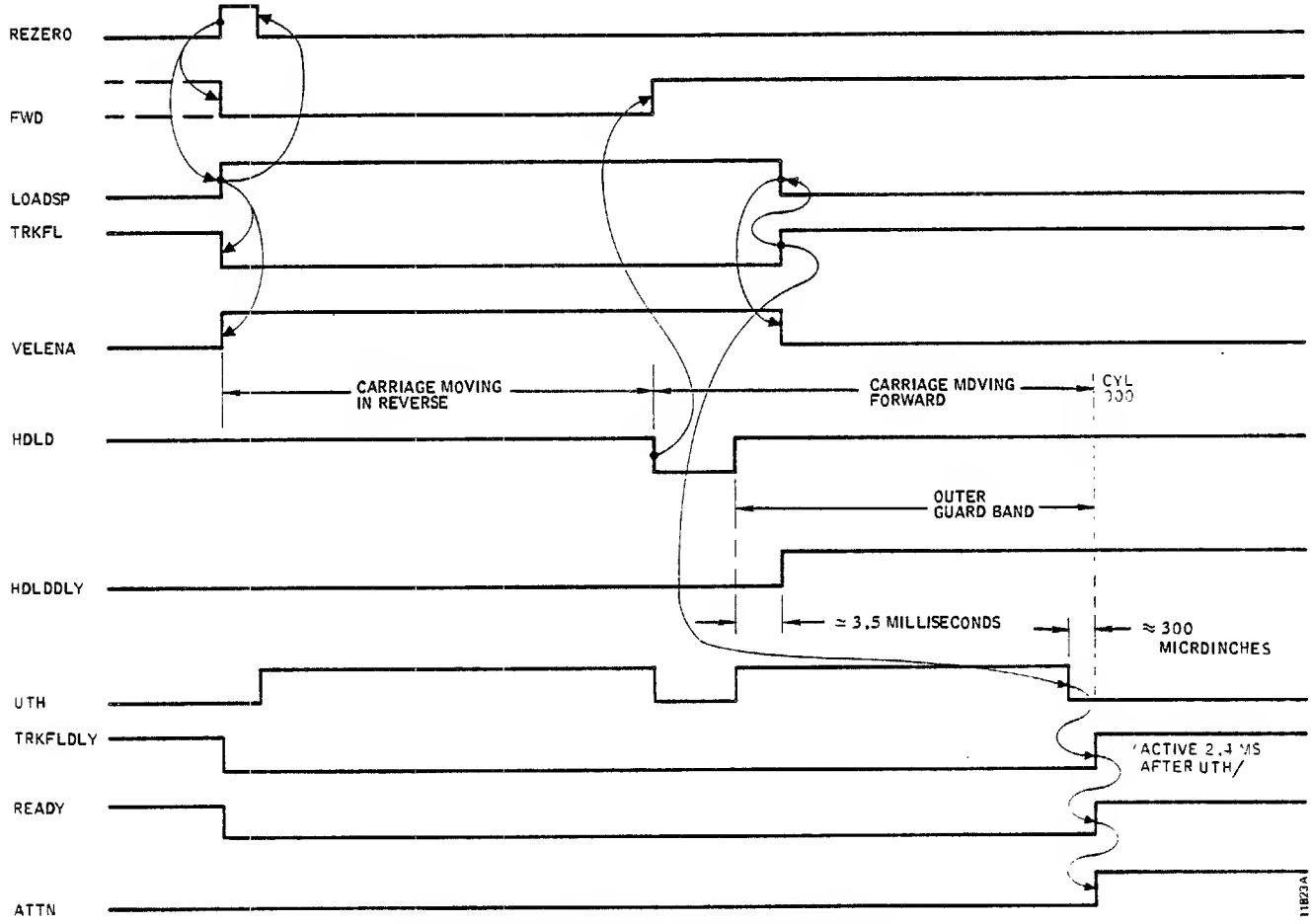

Figure 4-5. Rezero Drive Timing Diagram

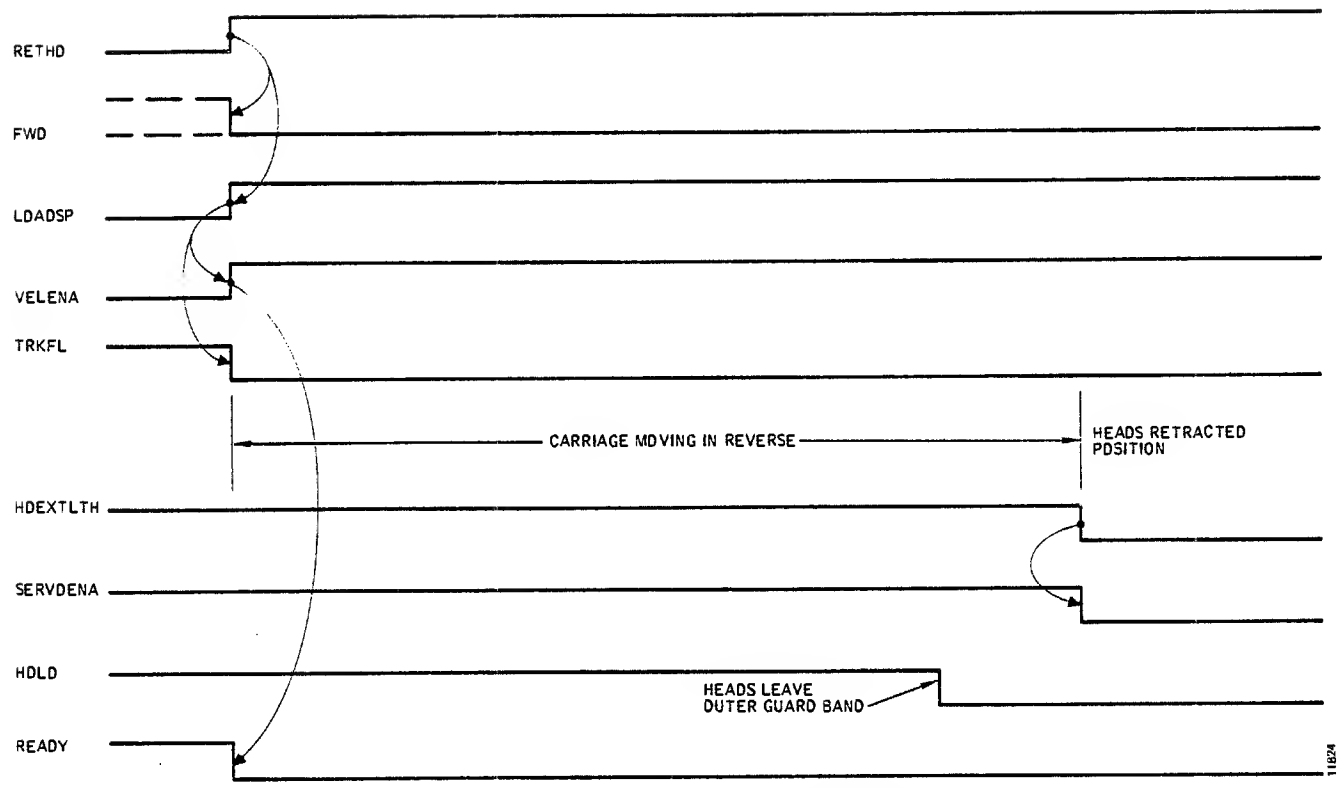

Figure 4-6. Head Retract Timing Diagram

Raising RETHD causes the FWD flip-flop to be reset and the LOADSP flip-flop to be set on the clock, raising VELENA to start the carriage moving in the reverse direction at load speed and causing the READY signal to fall. The TRKFL flip-flop is reset on the trailing edge of the next 1.6-megahertz clock. The READY line will stay low until the next head-load operation is performed and completed.

Head retract is completed when the carriage switches the Heads-Extended microswitch, dropping HDEXTLTH. When HDEXTLTH goes low, SRVOENA is dropped to disable servo drive.

SUBTRACTOR AND DIFFERENCE COUNTER

Programmed seeks require the calculation of a difference count between the cylinder address of the current head location (also called the old cylinder address) and the cylinder address after seek termination (also called the new cylinder address). This calculation is done by a 10-bit Subtractor, and the results of the calculation are stored in a 10-bit Difference Counter register. See Figure 4-7.

Old cylinder addresses are provided by Cylinder Address Register outputs CAR001 thru CAR512 to the A-inputs of the Subtractor. New cylinder addresses come from the controller over BUS 0 thru BUS 9 lines to the B-inputs of the Subtractor immediately before, during, and following the time that the Set Cylinder Tag line is activated. New and old cylinder addresses operate as minuend and subtrahend of the calculation, respectively, with the S-outputs of the Subtractor providing the nearly instantaneous difference between the two input values at all times.

Subtraction is performed as a 1's complement addition operation using standard full-adder circuits. To do this, the subtrahend must be inverted to 1's complement form, and the carry-out (CO) from the most-significant place must be fed back to the least-significant place carry-input (C1) of the adder. This carry wraparound completes the subtraction function.

Notice that the simplified logic of Figure 4-7 shows outputs CAR001 thru CAR512 applied to low-level true inputs of the Subtractor. In actual practice, the outputs of the CAR are inverted before being applied to the adder, in effect giving the required 1's complement subtrahend necessary for subtraction.

To understand the subtraction operation fully, consider the following simplified four-bit 1's complement addition examples:

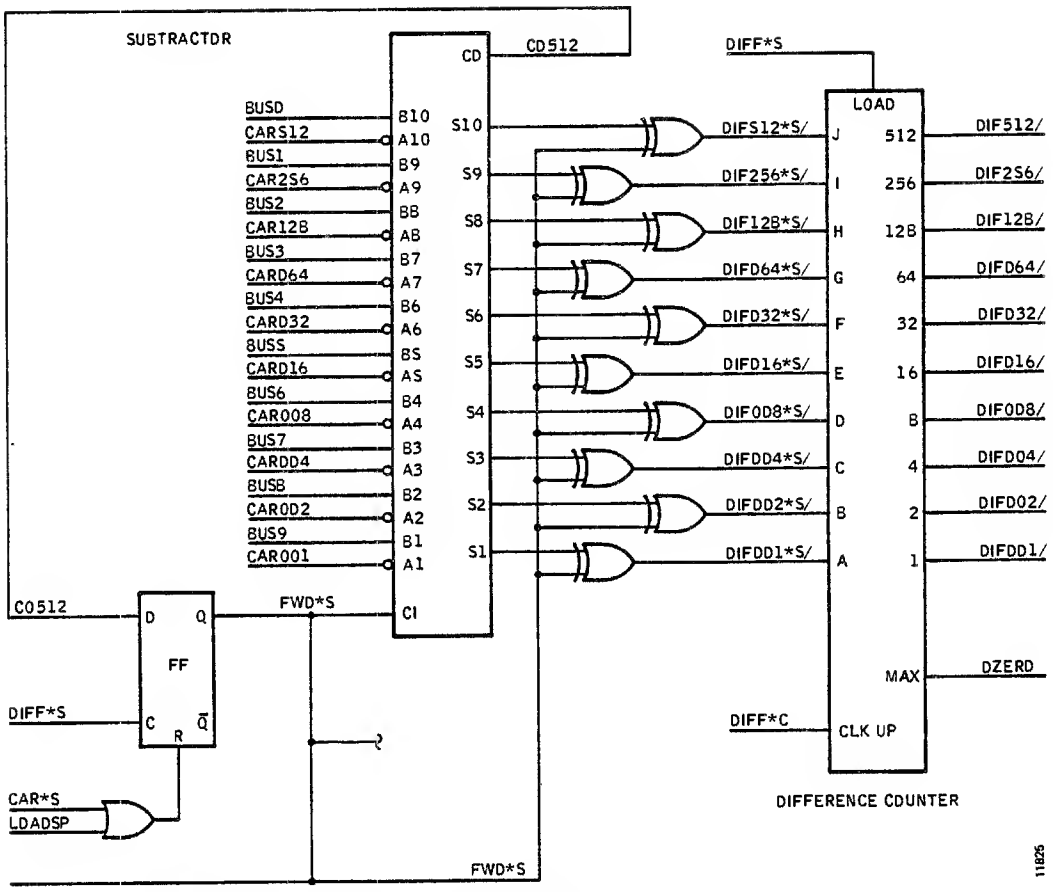

Figure 4-7. Subtractor and Difference Counter Logic, Simplified

- **Forward Seek (New Address Old Address)**

New Address
(BUS) = 5 = 0101

Old Address
(CAR) = $\underline{-2}$ = $\underline{+1101}$ (1's complement of 0010)
3 10010
1 (1's complement end-around carry)
0011 (difference)

- **Reverse Seek (New Address Old Address)**

New Address
(BUS) = 2 = 0010

Old Address
(CAR) = $\underline{-5}$ = $\underline{+1010}$ (1's complement of 0101)
-3 01100
0 (1's complement end-around carry)
1100 (1's complement of 0011)

Several basic rules of 1's complement addition can be concluded from the simplified example above: (1) all forward seeks, where the new address is greater than the old address, *always* generate a binary 1 end-around carry; (2) all forward seeks produce a difference output that is in normal form; (3) all reverse seeks, where the difference will be negative, will never generate a binary 1 end-around carry; and (4) all reverse seeks produce a 1's complement difference.

Returning to Figure 4-7, notice that the carry-out bit C0512 causes the FWD*S flip-flop to be clocked set by DIFF*S if the carry bit is a 1. FWD*S supplies the end-around carry to the carry in (CI) input of the adder, provides the direction input to the FWD flip-flop (not shown; see Figure 4-2), and activates the Exclusive-OR gate network that provides the inputs to the Difference Counter.

Recall that forward seek difference values are always in normal form and that reverse seek difference values are always inverted. The Difference Counter requires an absolute magnitude difference count; that is to say, if the difference between the two cylinder addresses is three, it wants to see a three, no matter what the sign. This is the function of the Exclusive-OR gates to invert positive-signal (forward) numbers loaded into the Difference Counter.

In the Trident logic design, it was chosen to load inverse (1's complement) numbers into the Difference Counter and to count up to a full count as the seek termination point rather than to load normal numbers

and to count down to zero. A quick look at the Exclusive-OR truth table that follows will show that the outputs of the Subtractor supplied to the parallel-load inputs of the Difference Counter are inverted when the FWD*S flip-flop is set and passed on without being inverted when FWD*S is not set.

FWD*S	Sn	OUT
0	0	0
0	1	1
1	0	1
1	1	0

The Difference Counter is parallel-loaded by DIFF*S signal from the Interface and Control System as a result of SETCYL being raised. Inputs may, and probably will, change while DIFF*S is present; but the stored, final difference count value will be the output of the Exclusive-OR gate when the DIFF*S load signal ends.

Once the Difference Counter is loaded, it is clocked to count up by track-crossing DIFF*C pulses as the carriage moves toward the selected cylinder. DZERO goes high when the Difference Counter reaches the full count state (MAX count). The changing DIF/ outputs of the counter control the changing values of D/A Converter voltages to the Servo System.

DIGITAL-TO-ANALOG CONVERTER

The digital-to-analog converter (DAC) used in Trident T200/T300 Disk Drives are based on a standard configuration of precision resistors that are connected to or removed from a summing junction by nine switching transistors (Figure 4-8).

The input gate logic determines the operational characteristics of the DAC according to the gate inputs. These characteristics are affected by the following factors:

- An active LOADSP signal when the heads are not loaded (HDLD/)

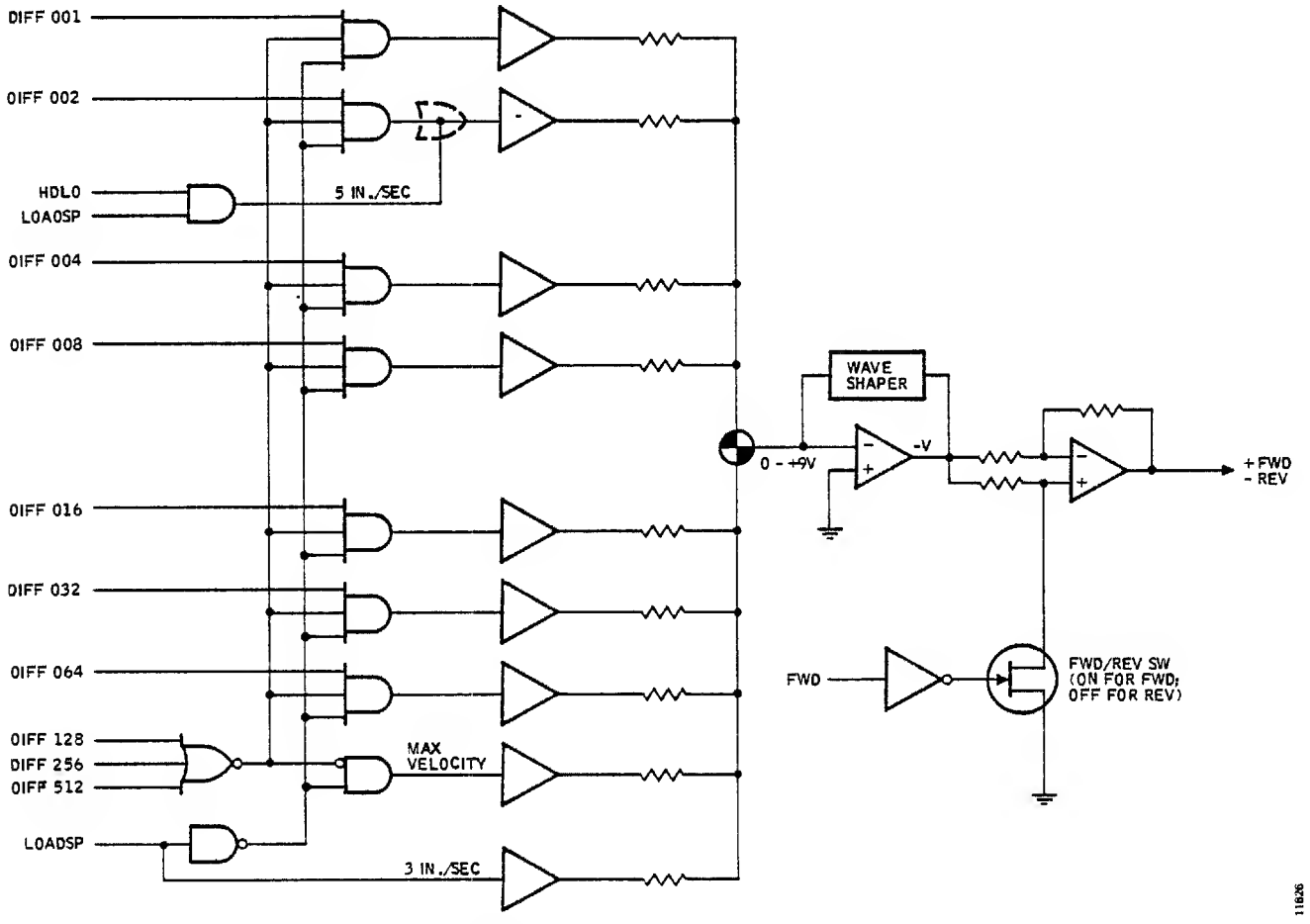

Figure 4-8. DAC Logic, Simplified

- An active LOADSP signal when the heads are loaded (HDLD)
- Cylinder differences greater than 127

Head carriage velocity varies according to whether or not the heads are loaded during a load speed operation. For example, at the start of a first-seek operation, before HDLD is detected, a single switching transistor is turned on, which causes the carriage to move at approximately 3 inches per second. After the heads are loaded and HDLD becomes active, a second switching transistor is turned on, which causes the carriage velocity to increase to approximately 8 inches per second. During a rezero operation, the same thing occurs when the carriage is driving in reverse and the HDLD signal is lost. Inputs to the gate logic are disabled whenever LOADSP is active.

Whenever the difference count exceeds 127 (i.e., number of cylinders to be traversed is greater than 127), maximum velocity is commanded from the DAC through a single switching transistor. All less-significant input gates are disabled until the count drops below 128, at which time the DAC will operate in a normal manner.

During seek operations where the difference count is less than 128, the precision resistors in the DAC sum the currents produced by the active DIFF001 thru DIFF064 signals to the input gates. Each resistor that is switched in adds an incremental voltage (or current) value at the summing junction that is equivalent to its bit weight. Conversely, when a resistor is switched out of the circuit, its bit weight is subtracted from the summation. A proportionate analog voltage (or current) is therefore present at the summing junction whenever one or more of the DIFF001 thru DIFF064 inputs is active.

The current flowing at the summing junction drives an op amp that incorporates a variable gain feedback loop commonly called the Wave Shaper. This circuit controls the profile of the acceleration ramp voltage that is later summed with the feedback voltage from the velocity transducer.

Forward-reverse polarity switching is done by switching the reference input of a second op amp to ground when the seek operation is forward. Input grounding is accomplished by a FET switch controlled by the state of the FWD signal. When FWD is active, the FET is turned on and the associated op amp sees a ground on the switch leg and a negative voltage on the other leg. The output of this op amp is therefore positive for forward drive. With the switch off, the negative voltage input to both legs of the amplifier produces a negative voltage for reverse drive.

SERVO DRIVE AMPLIFIER CONTROL

Figure 4-9 shows the circuitry that controls the servo drive motor amplifier. These circuits control the movement of the read/write heads during three different modes of operation:

- Velocity mode — During head load and unload operations (except the emergency retract operation), the DAC provides a fixed voltage output to the servo drive control circuits. During a program seek operation, the output of the DAC is variable. The manner of controlling the head carriage velocity is the same in both cases.
- Track-following mode — When the heads are detented on a cylinder track, the POSITION signal controls the drive amplifier.
- Offset mode — During an offset operation commanded by the controller, a fixed offset voltage is introduced into the servo system to cause it to move either forward or backward in an attempt to recover data.

During seek operations, the voltage from the DAC is summed at the input of the Velocity Amp with the output from a thermistor contained in the linear motor. This provides temperature compensation over the entire operating range of the machine. The voltage from the DAC may be the fixed level that determines load speed or the varying level that is proportional to the cylinder difference count. At the input to the Velocity Amp, it is always positive for forward movement of the heads and negative for reverse motion. The Velocity Amp is turned on by VELENA.

Movement of the linear motor coil causes the velocity tachometer to generate a bucking voltage (VELIN). The VELIN signal is applied to the feedback amp through a filter network that affords high-frequency pre-emphasis for quicker rise time response. The output of the feedback amp is a negative voltage of an amplitude that just matches the positive velocity control voltage at maximum forward seek speed. In other words, at maximum seek speeds, the output at the summing junction should be zero volt and the carriage should be in coasting mode. In practice, a small amplitude oscillatory condition will occur as the carriage slows down, reducing the VELIN signal, which allows the output from the DAC to regain control and increase speed again until the VELIN and DAC output voltages are equal.

During track-following operations, VELENA is inactive, and the head carriage position is controlled by the summation of VELIN and the POSITION signal. Even though the movements of the head carriage are minute at this time, the feedback amp is still an important and precise functional element of the control circuit.

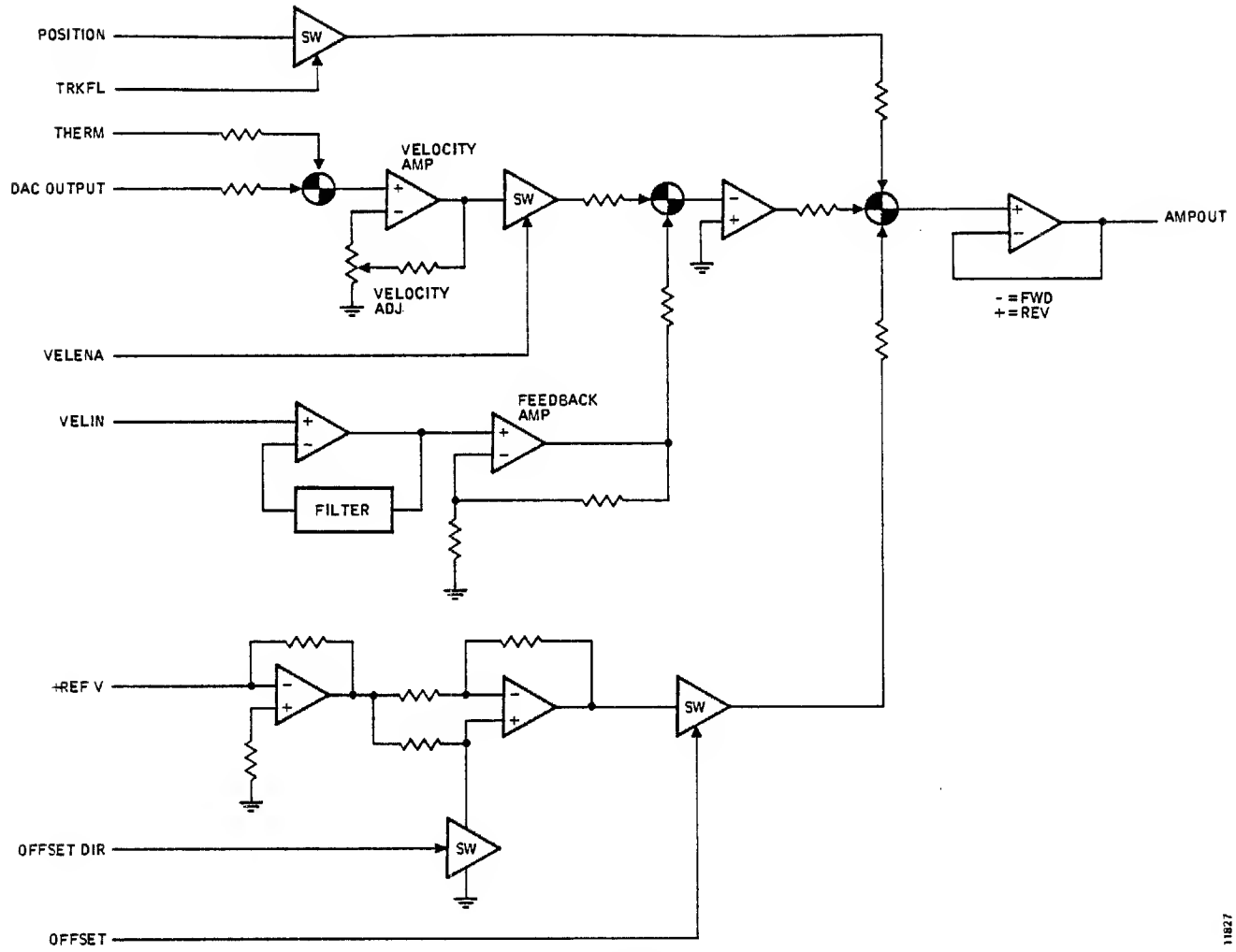

Figure 4-9. Servo Drive Amplifier Control Circuits, Simplified

The basic elements of the offset control logic are a reference amplifier, a direction amplifier, and two switches (Figure 4-9).

In the track-following mode of operation, the voltage at the summing point is nulled by the locking action of the servo system. When an offset operation is programmed, the offset control logic is switched into the circuit. This logic develops, at the summing point, an error voltage that causes the servo to make a false correction and thereby move the head carriage the correct distance off track for attempted data recovery.

The reference amplifier provides a precise minus input to both legs of the direction amplifier. Forward/reverse polarity switching is done by switching the reference input of the direction amplifier to ground when the offset operation is reverse. When OFFSET DIR is high, the switch is on and the amplifier sees a ground on the noninverting input and a negative voltage on the other leg. The output of the amplifier (error voltage) is therefore positive for reverse direction offsets. With the switch off (forward offset direction) the negative input voltage to both legs of the amplifier produces a negative error voltage.

DRIVE AMPLIFIER/LINEAR MOTOR

The servo drive amplifier and linear motor circuits are shown in simplified form in Figure 4-10. The servo drive amplifier provides positive or negative drive current to the linear motor as directed by the Amplifier Output (AMPOUT) of the servo drive control circuits.

Whenever an error voltage is introduced into the servo system, AMPOUT responds by swinging negative or positive according to the polarity of the voltage introduced. AMPOUT voltage deviations are sensed by a Switching Control circuit that provides a negative feedback and turns on either the positive or negative current switch. When either switch is on, a current path for the motor coil is completed; this allows the coil to drive the heads forward (positive voltage) or in reverse (negative voltage). Only one switch at a time is on, and whichever one is on switches approximately 50 volts directly to the motor coil.

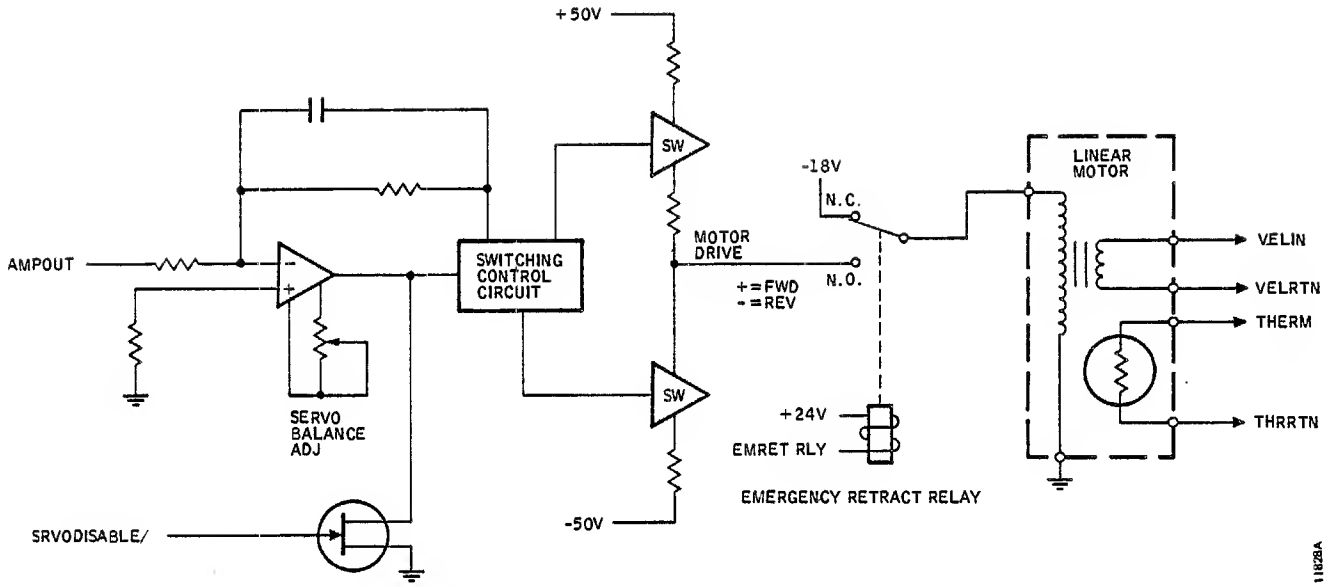

Figure 4-10. Servo Drive Amplifier and Linear Motor Circuits, Simplified

Although the ideal operational amplifier provides an exact zero-volt output when a zero-volt input is applied, this is not achievable in practice. Unavoidable mismatching of components causes these amplifiers to produce a dc offset when no input signal is present. The Servo Balance Adjustment shown in Figure 4-10 is adjusted to compensate for the offset produced by all the amplifiers in the servo system.

Note that the Motor Drive signal to the linear motor is applied through the contacts of the emergency retract relay. This allows the emergency retract operation to override servo control. This operation will be explained in a subsequent paragraph.

Housed within the linear motor case are the velocity transducer and a temperature thermistor. The thermistor develops a correction voltage that varies with the temperature inside the motor housing, and this correction voltage is included in the voltage summation during seek operations as previously described.

SERVO DISABLE LOGIC

There are certain times, for purposes of equipment protection, when it is desirable to disable the servo system. In addition to this, a number of events can occur, any of which may result in damage to the equipment if the heads are not withdrawn from the disk pack. The logic for disabling the power amplifier and for initiating an unscheduled head retraction is shown in Figure 4-11.

The SERVO ENABLE/SERVO DISABLE switch provides the CE with a means of disabling the servo for maintenance purposes. With the switch in the SERVO DISABLE position, the grounded SRVODISABLE/ line inhibits the operation of the power amplifier (see Figure 4-10). An emergency head retract (EMRET) operation when the servo is not disabled or a loss of the −18-volt supply for more than 2 seconds will disable the servo in the same manner. Conditions initiating an emergency retract operation will be discussed in detail shortly.

When power is first applied to the drive, the Power-On Servo Disable Clamp begins monitoring the −18-volt head-retraction voltage. During this time, the servo is disabled. After the delay, assuming that the −18-volt output is present, the clamp enables the switch for operation. The servo remains disabled, however, until SRVOENA goes active. This occurs when the first seek is initiated, which brings up SRVOENA.

An emergency retract operation removes the heads from the disk pack at approximately 30 inches/second and is initiated by any of the following conditions:

- A failure of either 50-volt circuit in the power (servo drive) amplifier
- A failure of any dc operating voltage
- Activation of the offrack switch (head carriage drives into the end stop)
- A SKENA command issued causing the heads to unload

Should either the +50- or −50-volt power circuits in the power amplifier fail and should this condition exist for 2 seconds or more, a valid failure is indicated and EMRET becomes active. The delay is employed to prevent false errors due to voltage transients, power bring-up delay, etc.

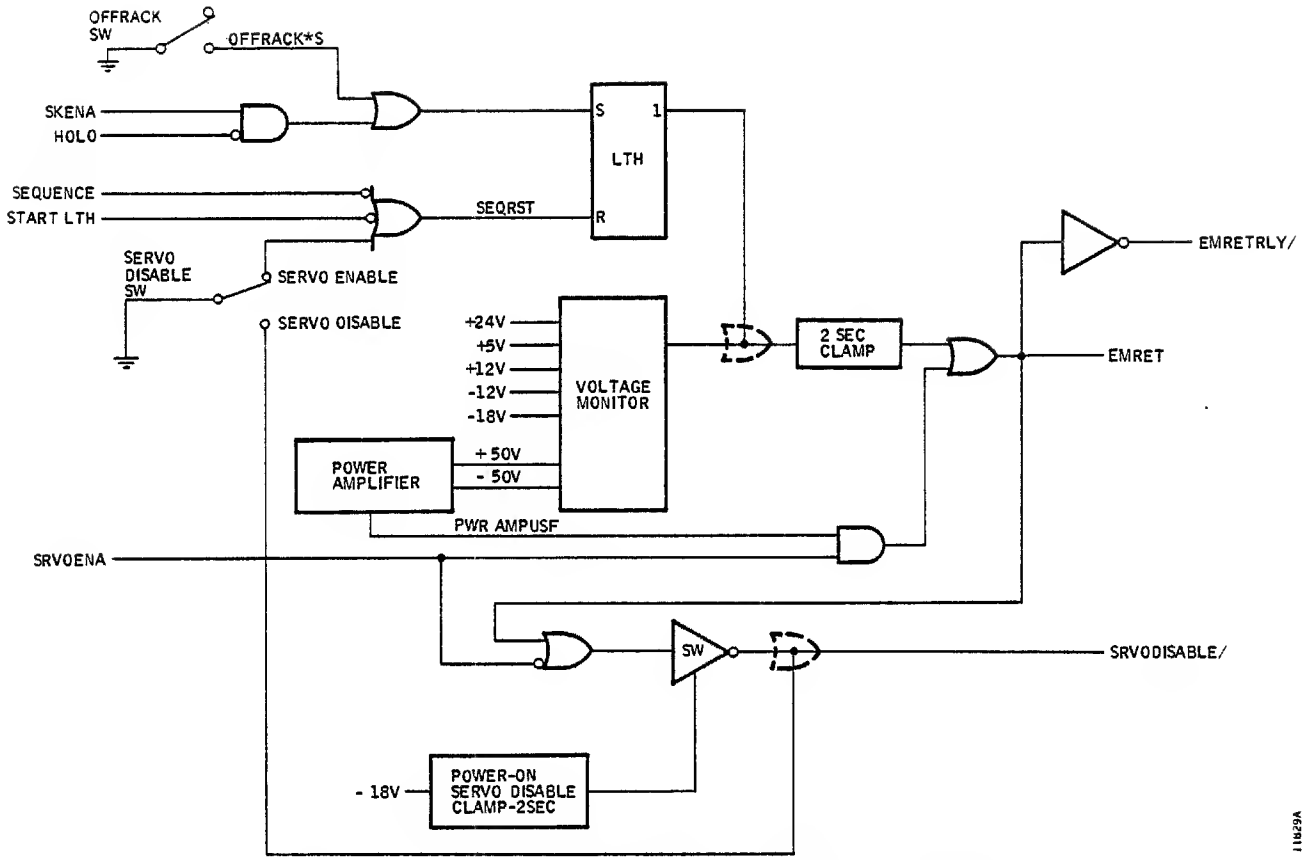

Figure 4-11. Servo Disable/Emergency/Retract Logic, Simplified

A monitor circuit within the power amplifier detects current to the linear motor. If one of the 50-volt servo drive circuits should short out, current would be supplied to the linear motor and the head carriage motion would be uncontrollable. The Power Amp monitor detects this condition and provides the PWRAMPUSF output. If the servo is not enabled (not under control) an emergency retract operation is initiated immediately; if the servo is enabled and under control, the chance of damage to the equipment is reduced significantly.

If the head carriage should drive into the end stop and thereby activate the offrack switch, or should a seek enable command be issued and the heads become not loaded, a latch will be set. The output of this latch initiates the emergency retract operation. Resetting this latch can be accomplished by any of the following actions:

- Sequence line dropped by the controller
- START/STOP switch set to STOP
- SERVO ENABLE/SERVO DISABLE switch set to SERVO DISABLE

Emergency retract operations are implemented by the emergency retract relay shown in Figure 4-10. EMRET is directed through a relay driver to de-energize the relay and in so doing cause a −18-volt driving voltage to be supplied through the linear motor coil. This results in a controlled head retraction at the maximum safe velocity.

DRIVE-READY AND OFFSET CONTROL LOGIC

The drive-ready condition occurs after a successful seek operation has taken place and while the read/write heads are detented on the selected cylinder. Logical elements involved in developing the READY signal are shown in Figure 4-12.

The Direction Control Flip-Flop controls the up and down direction of the count. Unless an offset operation is programmed, the counter operates as an up counter. When offsets are programmed, the counter counts in both directions.

At the beginning of each seek operation, VELENA goes active. This signal resets the Direction Control Flip-Flop, thereby setting up the counter for an up-count operation. It also sets the Load Latch, which in turn loads the counter with an all-zero preset count.

When VELENA is dropped at the end of the velocity mode and the Upper Threshold (UTH) signal falls as the servo enters the track-following mode, the Load Latch is reset. This action releases the counter load input and also enables the counter, since TRKFL is active and TRKFLDLY is inactive. An up-count operation begins at a 0.16-millisecond clock rate.

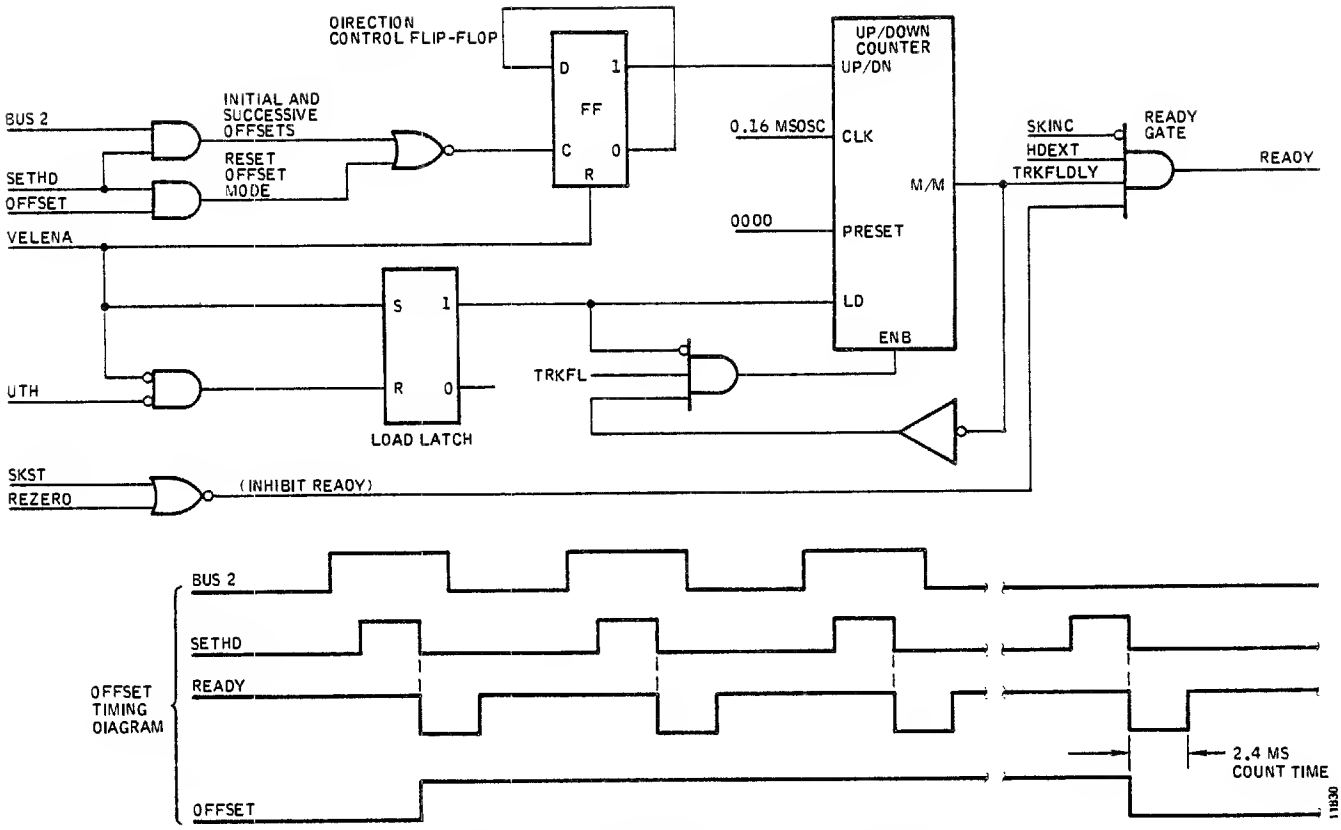

Figure 4-12. Drive Ready Logic, Simplified

After a 2.4-millisecond count time TRKFLDLY becomes active. Assuming that the seek operation is successful, SKINC will be inactive at this time and READY will be generated.

During offset operations, the generation of READY is controlled by the action of the Count Direction Flip-Flop. This prevents the controller from transmitting commands to the drive while the carriage is moving during an offset operation.

Offset operations normally comprise a sequence of individual and combined commands: for example, offset forward, offset reverse, offset forward and strobe early, etc. The sequence continues until the data is recovered or determined to be unrecoverable (hard error).

The controller initiates the offset sequence by transmitting a high level BUS 2 and the SETHD commands. As SETHD falls, the previously reset control flip-flop is set, which in turn programs the previously filled counter for a down-count operation. As the down-count commences TRKFLDLY falls, causing ready to drop. After 2.4 milliseconds, the counter is empty and TRKFLDLY goes active, bringing READY up again. The next offset command toggles the flip-flop, and during this sequence the counter counts up to a full count. This alternate count direction continues as long as the flip-flop is clocked. Refer to the timing diagram incorporated on Figure 4-12.

After the last offset operation has been completed, the controller transmits SETHD but does not raise BUS 2. This condition initiates an up or down count, as the case may be, just as described previously. The reason for the additional (last) SETHD command is to alert the controller to look at the new status; that is, the transition from (or resetting of) the offset mode of operation.

Some systems require an earlier detection of the fall of READY. This is accomplished with an OR gate that inhibits the Ready Gate as soon as a SKST or REZERO pulse occurs. This causes READY to fall somewhat sooner than it otherwise would, but the difference in time is negligible.

SEEK-INCOMPLETE DETECTION

Normal seek operations, other than those for extending and retracting the heads at load speed, require 55 milliseconds or less to complete. Seek time is measured from the instant that the unit drops the drive-ready signal at the start of a seek until the drive-ready signal is restored. If the seek operation is not completed within approximately 0.86 second, the seek-incomplete attention condition will be generated.

Figure 4-13 shows the logic, in simplified form, that detects seek-incomplete status. It is basically a modulo-16 up counter for counting 82-millisecond clock pulses from the Sequence Oscillator. The

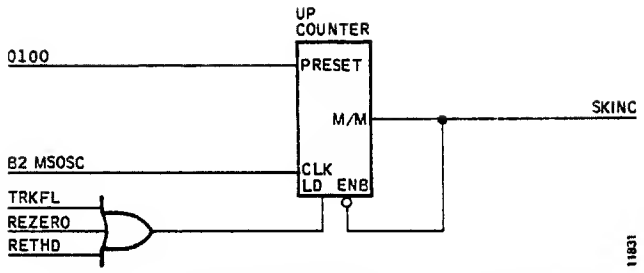

Figure 4-13. Seek Incomplete Detection Logic, Simplified

counter is preset with a count of four before the count operation, and a loading gate provides the counter control function. Note that the counter is always enabled for operation except when it has counted out a seek-incomplete operation.

Before a first-seek operation commences, RETHD is active, causing the counter to load the preset count. When the first seek begins, RETHD falls, thereby releasing the load input and allowing the count operation to start.

The count is normally interrupted when TRKFL becomes active at the end of the seek operation and reloads the counter.

Program seek operations begin with the counter preloaded, as described in the previous paragraph. When TRKFL falls, it releases the load input to start the count. At the end of a successful seek operation TRKFL comes up, reloads the counter, and thereby inhibits the count in progress.

An active REZERO signal also loads the counter. The count does not start until the REZERO pulse falls to release the load input. TRKFL then interrupts the count as previously described.

Should the count progress to completion, SKINC becomes active and disables the counter. A rezero or power-down sequence is then required to reload and thus enable the counter for operation.

SERVO SIGNAL PROCESSING

The servo surface dibit signals picked up by the read-only servo head are amplified by the Servo Preamplifier which comprises a two-state, low-noise differential amplifier circuit. See Figure 4-14. The dibit signals are processed to perform the following functions:

- Generate the POSITION signal that controls head carriage motion during track-following operations. This signal is also used to detect cylinder crossing.
- Generate the heads-loaded (HDLD) signal that indicates the heads are loaded on the disk pack.

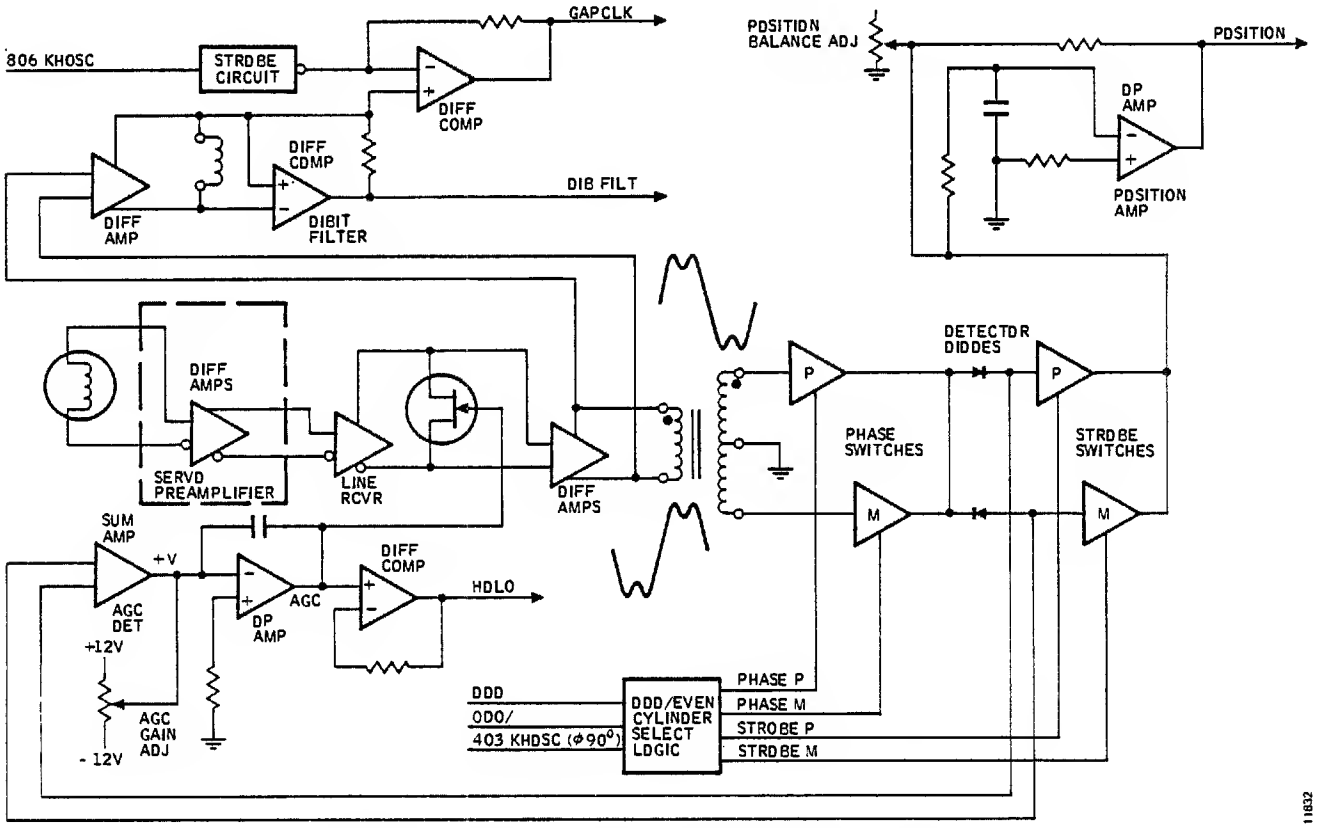

Figure 4-14. Servo Signal Processing Logic, Simplified

- Generate the gap clock (GAPCLK) signal that is used to detect the physical index mark on the disk pack

- Provide a filtered dibit signal (DIBFILT) that is used to sync the VCO

Outputs from the Servo Preamplifier are impedance matched to the processing circuits by a line receiver. After further amplification, the dibit signals are applied to a step-up pulse transformer. The secondary of the pulse transformer has a grounded center tap so that it provides two outputs that are symmetrically identical but differ in phase by 180 degrees.

Each leg of the secondary has a phase-select switch, a detector diode, and a strobe switch. All four FET switches are controlled by the odd or even cylinder select logic. The odd or even cylinder select logic determines which switches should be on depending upon the odd or even nature of the selected cylinder. The purpose of this odd or even selection, as explained earlier, is to ensure that the polarity of the resulting POSITION signal is correct to drive the detented heads toward the center of the cylinder. This is true regardless of undershoot or overshoot conditions.

The selection logic compares the ODD and ODD/ (even) signals with the 403KHOSC clock signal that has been phase-shifted by 90 degrees. See Figure 4-15. Notice the following:

- The PHASE P switch is turned on for an even cylinder selection, and the PHASE M switch is turned on for an odd cylinder selection.

- The STROBE P and STROBE M switches are turned on 180 degrees out of phase with each other.

- The polarity of the strobe switches is switched 180 degrees between even or odd cylinder selections.

The inverted or noninverted dibit signal selected by the phase switch that is turned on appears at the diode junction. One diode detects the positive signal components, and the other detects negative signal components. These positive or negative voltages are then passed on to their respective strobe switches.

The strobe switch phasing is such that the STROBE P switch samples the second half of the positive dibit signal peaks and the STROBE M switch samples the second half of the negative dibit peaks for even-numbered cylinders. See Figure 4-16. The opposite is true for odd-numbered cylinders.

Signal integration occurs at the input to the POSITION amplifier. The voltage peaks are converted to positive and negative voltage levels proportional to the sampled dibit signals. When the dibit signal is symmetrical, the two opposing levels are equal and cancel

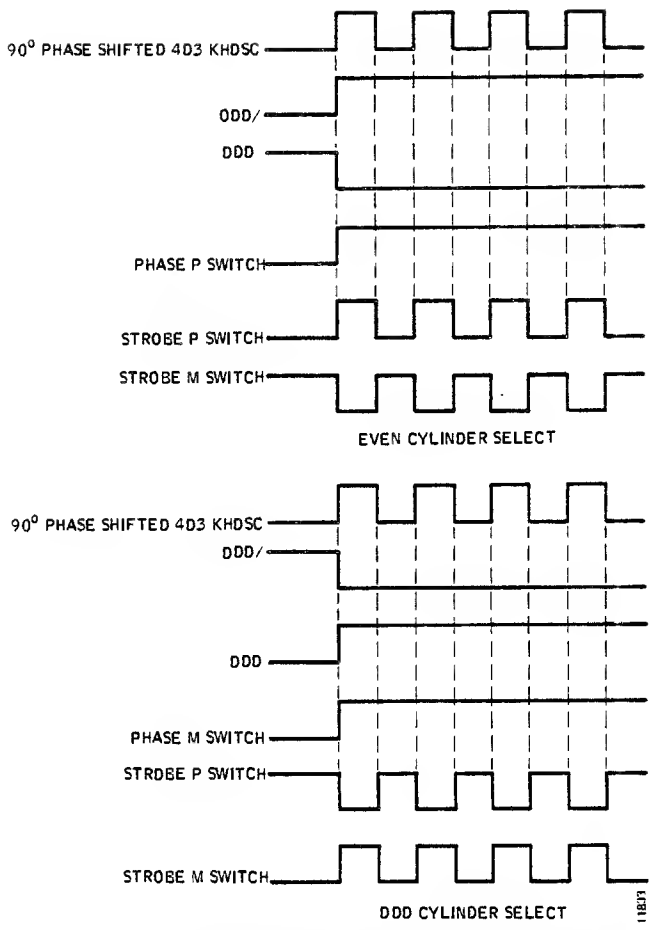

Figure 4-15. Odd/Even Cylinder Phase and Strobe Signal Comparisons

each other out, resulting in a null input to the POSITION amplifier.

A POSITION signal is generated whenever the summation of STROBE P and STROBE M switch outputs is not zero. If the summation goes positive, the POSITION signal goes negative, causing the heads to move in the forward direction. A negative summation summarily causes head movement in the reverse direction. A balance control at the summing input permits minor adjustments to be made to correct for circuit dissymmetry.

During forward and reverse seek operations to new cylinder positions, the POSITION signal swings positive and negative in a sinusoidal manner. Advantage is taken of this characteristic in detecting track crossings that correspond to the null points where polarity reversal of the POSITION signal occurs. See Figure 4-17.

Notice in the figure that several examples of short seek operations are given. The differences observed between the examples occur because of the plus and minus patterns present under the servo head at the starting cylinder position and because of inversion or

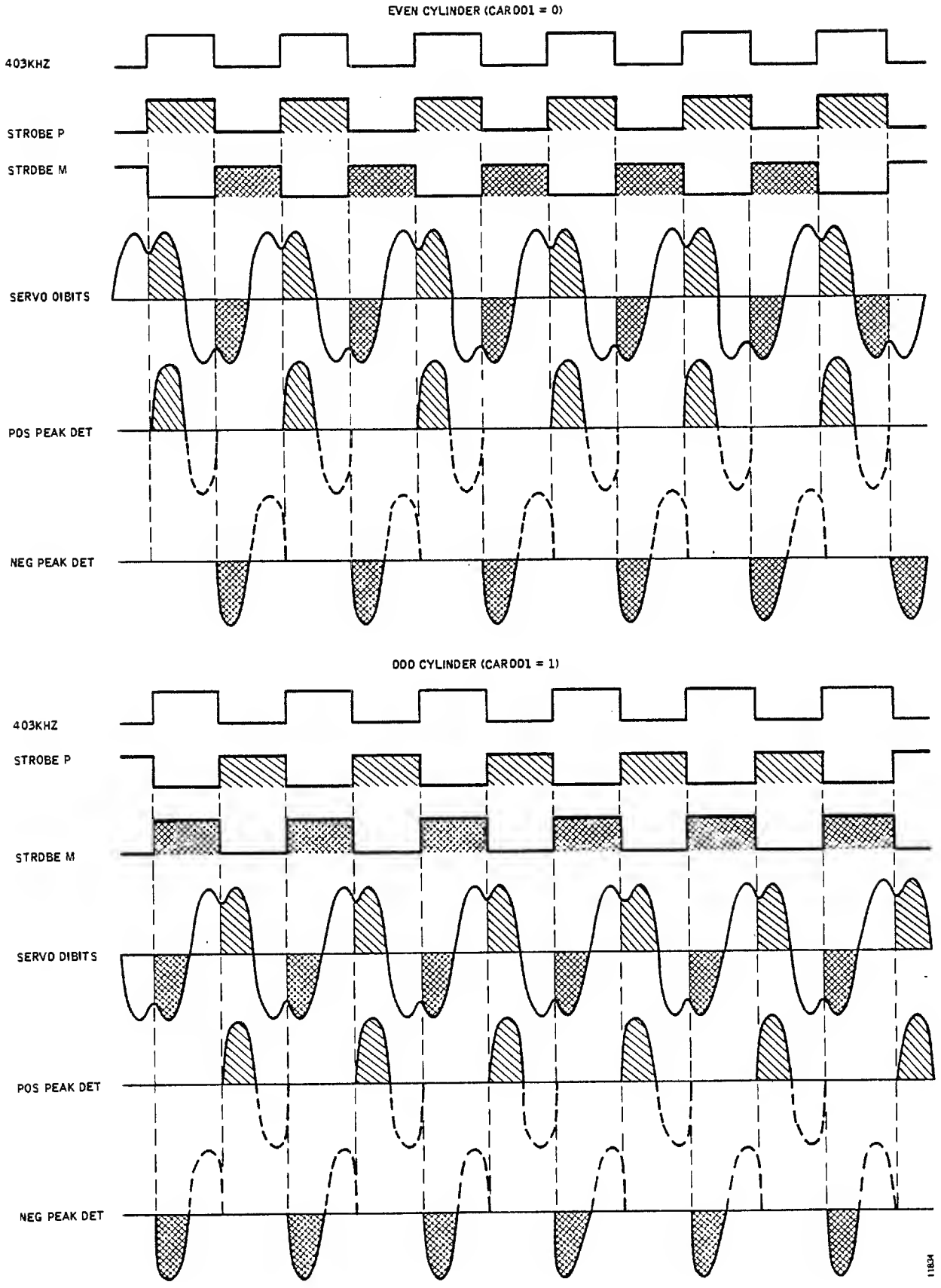

Figure 4-16. Dibit Peak Detection Timing Diagram

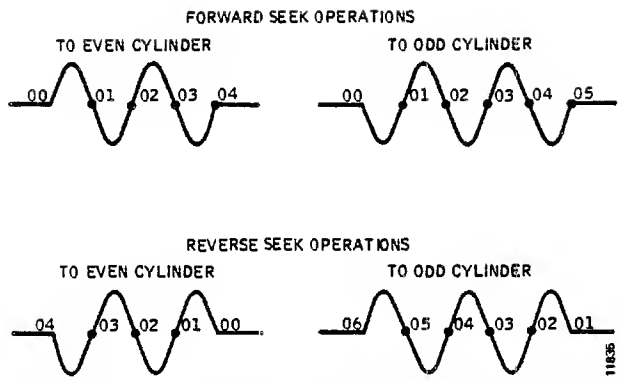

Figure 4-17. POSITION Signal Polarity Control

noninversion of the resultant dibit signal when seeking to an odd or even cylinder.

Regardless of polarity, the track crossings represented by the POSITION signal during a seek operation are used to generate the clock for the Difference Counter, as described under the next heading.

The dibit output of the servo head is not constant because of the difference in rotational velocity between the inner and outer cylinders and because the height that the head flys above the disk varies somewhat. An automatic gain control (AGC) circuit compensates for these differences. The circuit consists of a summing amplifier, an integrator amplifier, an FET shunt, and a gain adjustment potentiometer.

The summing amplifier sums the dibit signals from the detector diode outputs and provides the summation output to an integrator amplifier. The integrator amplifier averages out the summation, and this voltage controls an FET shunt that is connected across one of the differential amplifiers. As the applied voltage becomes higher, the shunting effect becomes greater and vice versa. The gain control varies the gain of the integrator amplifier and, thereby, controls the total gain.

The AGC voltage is monitored by a differential comparator circuit. When the heads are not loaded, no AGC voltage is developed and the circuit is biased off. As the heads cross the outer guard band during an initial load operation, the AGC voltage is generated, and this voltage overcomes the bias voltage. The comparator senses the input change and produces the heads-loaded (HDLD) signal.

Two other signals are derived from the servo head dibits; dibit filter (DIB FILT) and gap clock (GAPCLK). DIB FILT is generated by a differential comparator that senses the dibit signal taken from the primary side of the center-tapped transformer. It tracks the dibit signal exactly and is used to sync the phase-locked oscillator (PLO). GAPCLK is generated by a differential comparator that senses the missing dibits at index time.

UPPER THRESHOLD AND DIFFERENCE CLOCK GENERATION

The POSITION signal, derived from the Servo head dibit signal, is monitored by a circuit that detects signal amplitudes above certain threshold levels. This Upper Threshold Detector circuit consists of a pair of operational amplifiers — one for positive and one for negative swings in signal polarity — whose outputs are combined by additive gating to provide upper threshold signal UTH.

Notice in Figure 4-18 that the active inputs to which the POSITION signal is applied to the two operational amplifiers are both noninverting, but that the amplifiers are biased with opposing voltages. The amplifier that produces UTP is turned on by positive signal transitions, and the amplifier for UTM is turned on by negative (minus) transitions. The threshold bias levels applied to the reference inputs of the operational amplifiers are such that one or the other will be turned on when a ± 0.75-volt amplitude of the POSITION signal indicates that the heads are 500 microinches off track center. Positive feedback prevents the amplifiers from being turned off until the amplitude of the POSITION signal drops below ± 0.20 volt for a head position of 130 microinches off track center.

The upper threshold signal is used in the Status and Error Detection system logic to detect off-track write errors.

UTH signals are processed further to produce the Difference Clock pulses required to decrease the count in the Difference Counter during cylinder seek operations. Recall that during seeks, the POSITION signal swings in a sinusoidal pattern with an amplitude of plus or minus 2 volts with 0-volt crossover points at track center. This can be seen in Figure 4-19.

Consider what occurs during a four-cylinder forward seek from cylinder 00 to cylinder 04, as shown on the left-hand side of Figure 4-19. Because FWD is high and DIFF001 is low, the SKST pulse that starts the seek operation will reset the four flip-flops, FFA thru FFD, in the Difference Clock Generator. The difference count will be set at four.

As the heads move from Cylinder 00, the POSITION signal increases in the positive direction, and UTP is turned on when the threshold level is reached. The rising edge of UTP sets flip-flop FFA, which enables FFB to be clocked set by the next 403KHZ clock pulse. FFC and FFD are turned on in succession by the next two 403KHZ clock pulses. An Exclusive-OR gate monitors the FFC and FFD outputs and produces a short DIFF*C pulse during the time that FFC is set until FFD is set. This clock pulse reduces the difference count to three, turning on the DIFF001 odd-even bit.

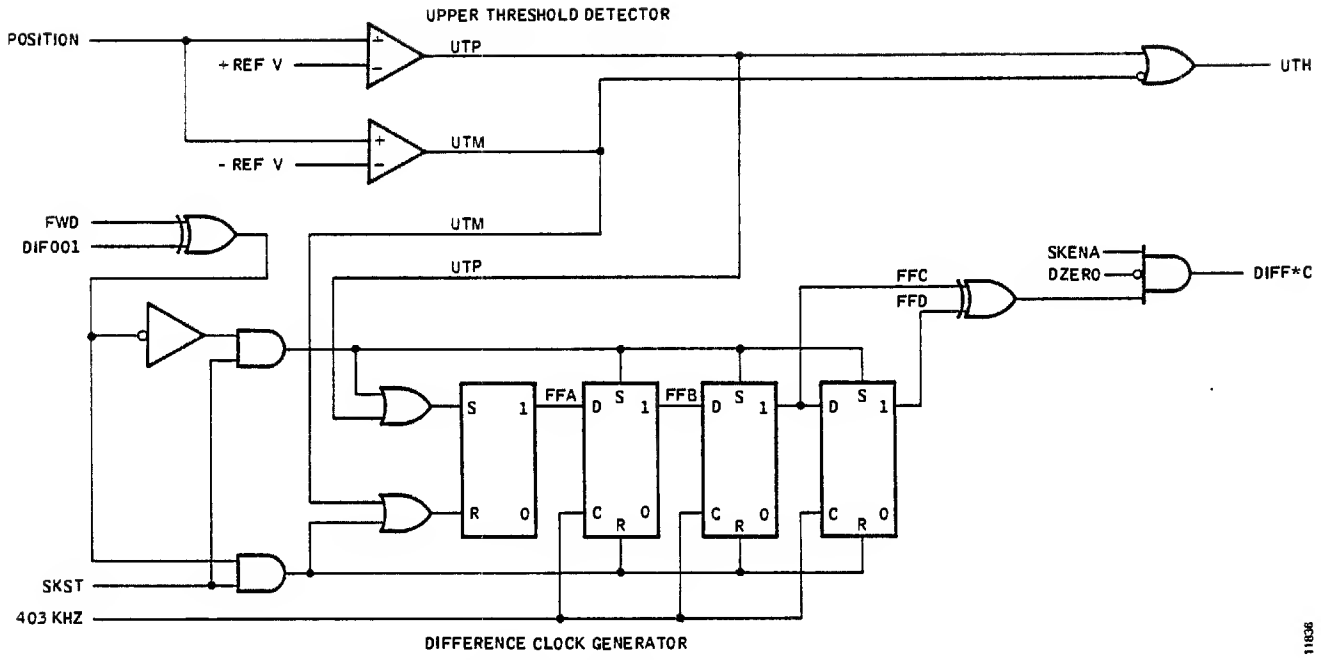

Figure 4-18. Upper Threshold and Difference Clock Circuits, Simplified

As the heads approach Cylinder 01, the POSITION signal decreases until it drops below the threshold level to turn off UTP. At track center of Cylinder 01, the POSITION signal swings negative and turns on UTM when the negative threshold amplitude is reached. The leading edge of UTM resets FFA, which is propagated to FFB, FFC, and FFD by successive 403KHZ clock pulses. Another DIFF*C clock pulse, produced during the time that FFC is reset before FFD is reset, reduces the count to two.

This process of detecting UTP and UTM signals from the polarity and amplitude of the POSITION signal is repeated once more in a four-cylinder seek to produce two more DIFF*C clock pulses, which reduce the difference count to zero. Notice that Upper Threshold Detector output signal UTH is a composite of signals UTP and UTM.

A four-cylinder, reverse-seek operation is similar, as shown in the right half of Figure 4-19. Notice however, that, because FWD and DIFF001 are both low at the start of this operation, SKST will set all four Difference Clock Generator flip-flops as their initial condition. In this case, UTM, which occurs first due to the negative initial swing of the POSITION signal, resets FFA; UTP, which occurs later, sets the flip-flop again. All other conditions remain the same.

The SKENA and DZERO inputs to the Difference Clock Generator output gate are qualifying terms. They allow the generation of difference clocks only if a programmed seek is taking place and then only until the difference count reaches a count of zero.

PHASE-LOCKED OSCILLATOR

A voltage-controlled oscillator generates the PLO pulses at 6.45 megahertz (T200) or 9.67 megahertz (T300) used by the Read/Write system to synchronize write-data timing. The output of the oscillator is phase locked to the dibit signal read from the disk pack servo surface when the heads are loaded. This oscillator also produces the basic clock pulses used by the drive at 1.6 megahertz, and at 806 kilohertz, 403 kilohertz, and 12.6 kilohertz. These clocks are derived by frequency division of the oscillator output. See Figure 4-20.

Notice in Figure 4-20 that the phase-lock loop is completed by bringing the 403KHOSC clock signal to a phase comparator circuit for phase comparison with the DIB FILT signal from the servo signal processing logic. This signal reflects the dibit signal exactly.

The flip-flop phase comparator provides two output frequencies depending upon whether or not the heads are loaded. If the heads are not loaded, the flip-flop toggles and provides a symmetrical pulse train output frequency of 201.5 kilohertz. If the heads are loaded, the output frequency is 403 kilohertz. However, the output may be symmetrical or it may not. The symmetry of the output waveform is the basis for developing a correction voltage.

When the heads are not loaded, the symmetrical 201.5 kilohertz pulse train output is averaged out by the integrating capacitor. This average voltage level is

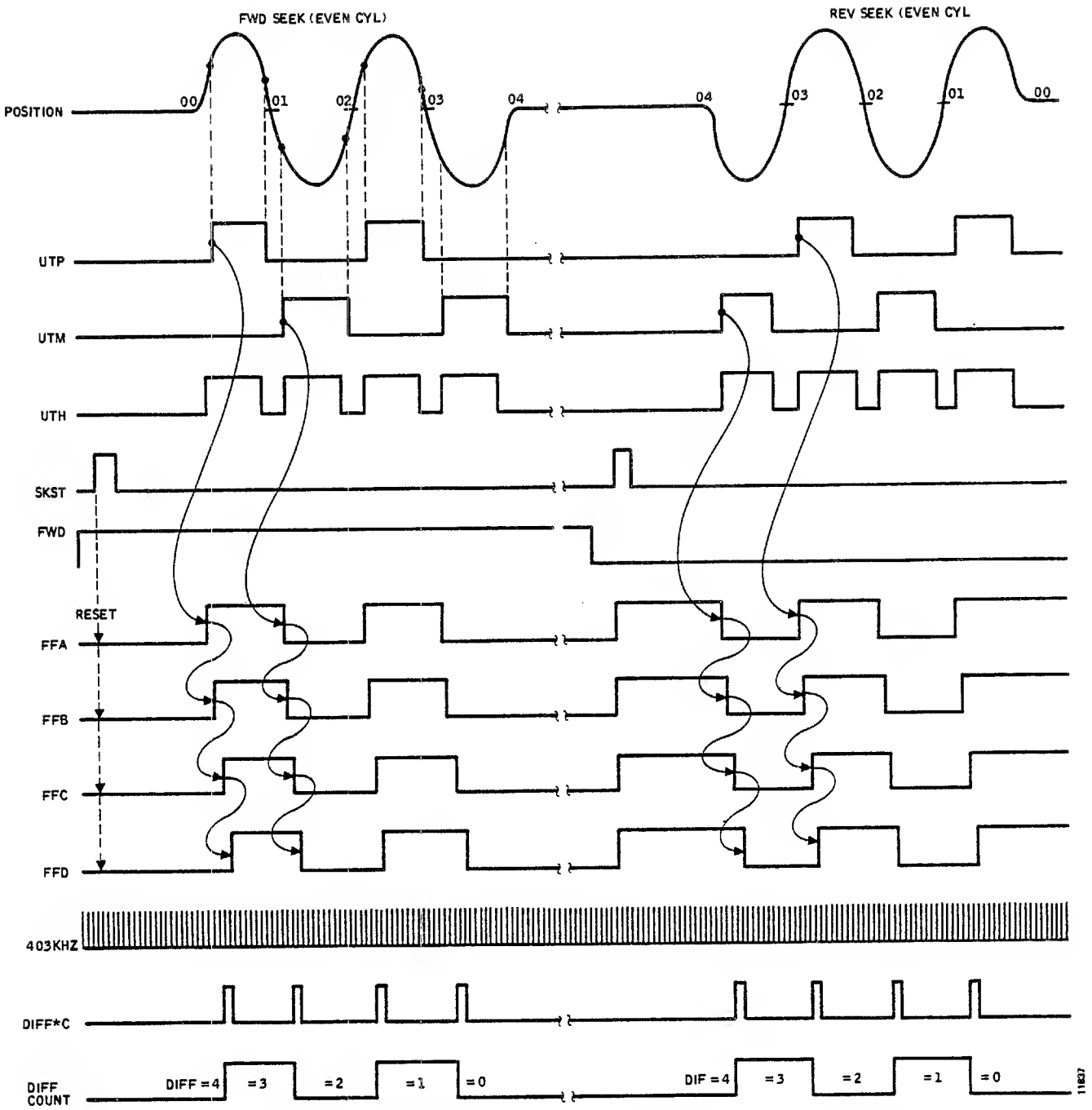

Figure 4-19. Upper Threshold and Difference Clock Timing Diagram

correct for maintaining the PLO output at a 6.45 megahertz rate (T200) or at a 9.67 megahertz rate (T300).

When the heads are loaded, the DIB FILT signal developed by the servo signal processing circuits becomes active. The 403KHOSC and DIB FILT waveforms are identical (see Figure 4-21); they differ only in phase. Ideally, this difference should be exactly 180 degrees. DIB FILT is sensed by a gate trigger that produces a narrow pulse with each negative excursion of the DIB FILT signal. When the phase difference is exactly 180 degrees, the gate trigger resets the flip-flop and changes the output frequency to a symmetrical pulse train of 403 kilohertz. The integrating capacitor averages out the 403 kilohertz output and produces an average voltage level that is the same as the voltage level produced by the 201.5 kilohertz signal when the heads are not loaded.

Should the DIB FILT and 403KHOSC signals differ by a phase angle other than 180 degrees, a correction is required. Figure 4-21 shows two examples, one with DIB FILT leading the 403KHOSC signal, and the

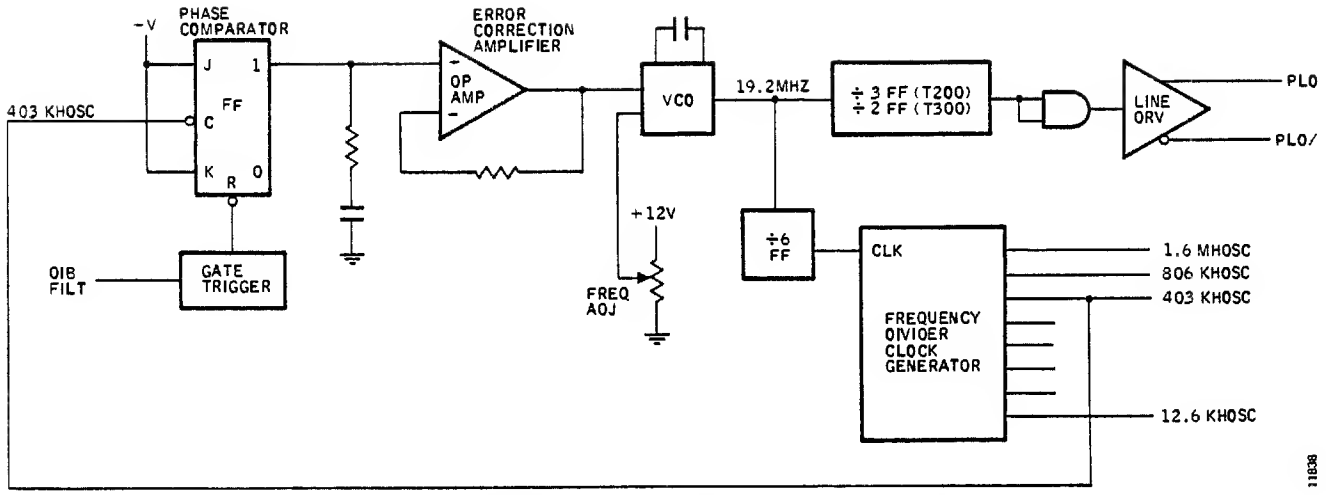

Figure 4-20. Phase Locked Oscillator Circuits, Simplified

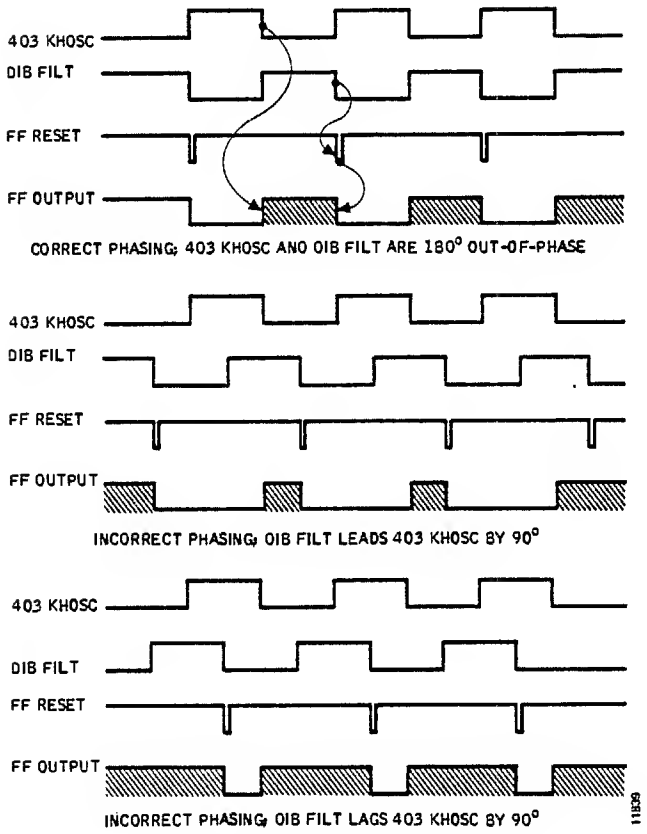

Figure 4-21. Phase Comparator Output Timing Diagram

other with DIB FILT lagging in phase angle. Notice in both cases that the effect of the lead or lag is a change in the reset timing of the flip-flop, which in turn effects the length of time that the flip-flop remains set. Since the output waveform in both cases is asymmetrical, the average voltage developed by the integrating capacitor is either more or less than the ideal average, and the difference is the actual correction voltage.

The Error Correction Amplifier and its associated circuitry (not shown) amplify and filter the voltage developed across the integrating capacitor. This arrangement compensates for slow frequency and phase variation and doesn't respond to instantaneous changes.

The voltage-controlled oscillator (VCO) is designed for a free-running frequency of 19.2 megahertz. The frequency of the oscillator is determined by the external capacitor, the voltage control input from the Error Correction Amp, and the frequency range control from the Freq Adj potentiometer. In actual practice the potentiometer setting locks in the pull-in range of the VCO.

The VCO output is divided down by flip-flop divider networks to provide the PLO pulses and to clock the frequency divider counter. Two different dividers are used to develop the 6.45 megahertz PLO pulses; a divide-by three circuit is used in the T200, and a divide-by-two circuit is used in the T300. A single divide-by-six circuit develops the clock signal for the Frequency Divider Clock Generator.

An eight-bit binary counter performs the clock generator function by further frequency division. These clocks are the basic timing signals used throughout the disk drive.

SECTION 5
READ/WRITE SYSTEM

This system contains logic for read/write head selection, for processing NRZ write data into peak-shift compensated TFM write signals, and for recovering NRZ read data from the TFM read signal. It also contains a Voltage-Controlled Oscillator (VCO) that provides read/write clock pulses to the controller for strobing read data, and for switching the write data line.

Figure 5-1 shows the primary components of this system. They include:

- Head Select Decoder
- Data Encoder
- Peak Shift Compensator
- Selectable Write Current Source
- Write Drivers
- Read Preamplifiers and 90-Degree Phase Shift Amplifier
- Crossover Detector and Digitizer
- Skew One-Shot
- NRZ Code Generator
- Address Mark and Read Sync Logic
- Voltage-Controlled Oscillator (VCO) Clock System

One of the nineteen read/write heads is selected for operation by decoding the binary count in the Head Address Register when the Head Select line is active. This is done by the Head Select Decoder that provides a head enabling ground return on the line to the appropriate head.

A write command from the Interface and Control System activates the write data line receiver; this permits NRZ write data from the controller to pass to the Data Encoder.

PLO pulses from the Head-Positioning Servo System are gated to the VCO system at this time by the inactive state of the READ signal. This ensures that the VCO system will be phase locked to the servo head signal while the read/write clock is transmitted to the controller.

Trident Model T300 Disk Drives employ a Peak Shift Compensator wherein a pattern of bit intervals is analyzed to determine whether or not an individual bit should be written early, late, or on time. The logic for making and implementing this decision is incorporated in the compensator itself. Peak shift compensation is not used in the Trident Model T200 Disk Drive.

Miller pulses from the encoder are shifted serially into the compensator (T300 only). After the appropriate timing has been determined, the data is clocked out to the Write Flip-Flop and then to the Write Driver.

A selected Write Current Source provides write current to the Write Driver when the data pulses turn the driver on. The three most-significant bits of the address in the Cylinder Address Register control the current supplied to the write driver by stepping the current down in increments for every 128-cylinder increase. This is done to compensate for the decrease in head-to-disk spacing, bit crowding, and other factors as the heads move inward toward the hub. Write current passes through only the head selected by the enabling ground return line.

If address mark variable-length sectoring is used, a Write Address Mark command from the Interface and Control System will turn off the Write Driver for an interval of 3 bytes (24 bits). An Address Mark Detector is triggered by this 3-byte gap when data is read back; this sends an Address Mark Detected signal back to the Interface and Control System for status output to the controller.

A read command from the Interface and Control System activates the read data line driver, thereby permitting NRZ read data from the NRZ code Generator to be transferred to the controller. The read command also performs the following functions:

- Enables the read data output of the Crossover Detector except during an address mark search
- Connects the VCO system to the read data so that the read/write clock transmitted to the controller will be synchronized to the data

The raw read signal picked up by the selected head is amplified by the read preamplifiers and phase shifted 90 degrees (differentiated) so that zero-crossing points of the signal correspond to TFM transitions. A Crossover Detector recovers the TFM data by switching on and off every time the read signal passes through the 0-volt axis. A digitizer converts the TFM data into Miller code by generating a narrow output pulse for every change in the TFM signal. The Miller read data is sent to the VCO system as a sync reference during reading and to the Skew One-Shot for further processing.

The Skew One-Shot is used for final positioning of read data in the center of the data window and also

permits the data to be strobe-shifted early or late during controller attempts to recover from read data errors. The data is then passed to the NRZ Code Generator for read clock synchronization and conversion to NRZ code and sent to the read data line driver.

The VCO clock system that produces PLO or read data synchronous clocks for the entire Read/Write System consists of a Phase Detector, the VCO, and a Divider and Clock Generator circuit.

The Phase Detector is actually a phase comparator that produces a control voltage to speed up or slow down the VCO. The detector inputs vary according to the operation being performed;

- Write operations require the PLO and 2F clock signals.
- Read synchronization requires the Miller read data and phase clock signals.
- Read operations require the Miller read data and the 2F clock signals.

During a write operation, the VCO is locked to the prerecorded servo signal picked up from the disk surface (PLO). This provides a stable reference for the recording operation.

When the read operation is initiated, the selected read head begins picking up data immediately, but the data is useless until it can be synchronized with a clock signal. The track record contains a VFO lock field that follows the preamble (sector format) or an address mark (address mark format). When this field is read, the Phase Detector sees the all-zero VFO lock pattern and the phase clock. This clock enhances the ability of the Phase Detector to shift phase very quickly so that the VCO phase can be corrected more quickly than under normal conditions.

After the VFO lock period has passed, the read sync clock input is replaced by the 2F clock so that the record identification can be read. A VFO relock time is then initiated with the phase clock again becoming active. When the relock time has passed, the 2F clock replaces the phase clock input for the actual reading of the record.

The VCO output is a square wave varying around a free-run frequency of two times the bit rate frequency (2F). This 2F frequency is divided down by the Divider and Clock Generator to the bit-rate frequency (F) that also serves as the read/write clock sent to the controller and NRZ clock signals. The read/write clock rate is 9.67 megahertz (T300 or 6.4 megahertz (T200). The NRZ clock times the read data so that transitions occur at the center of the bit-cell time and coincide with the falling edge of the read/write clock.

The Address Mark and Read Sync Logic generates and detects the 3-byte address mark and provides a read-synchronization-enable signal during VFO lock and relock periods. Simultaneous write and address mark commands prevent write data from reaching the Write Flip-Flop for a period of three byte intervals to cause an address mark to be written.

During an address mark search operation, the read and address mark commands are both brought up, and the subject logic begins monitoring the read data. When the address mark gap is detected, an enabling output is directed to the Divider and Clock Generator, which in turn provides the phase clock signal to the Phase Comparator. Timing for the read synchronization is developed internally by the logic under discussion. Data to the controller is inhibited during the VFO lock and relock periods regardless of the track format used.

HEAD SELECT AND DRIVE MATRIX

The binary address (HD08RM-HD01RM) from the Head Address Register is converted to a decimal number by a 4-to-10 line decoder (Figure 5-2). A ground output from the decoder enables the selected head for operation. The right matrix illustrated in Figure 5-2 selects 10 heads and the left matrix selects nine. The tenth head on the left matrix is a dummy head; its function will be explained later. Head-select circuits are identical for all heads.

A matrix of 76 diodes (four per active head) connect the outer leads of each head winding to write-drive and read-sense lines shared in common. The polarity of the matrix diodes is such that +24 volts on the select lines of unselected heads back-biases the diodes, effectively decoupling the heads from read or write activity. Conversely, the ground level on the selected head provides a return path for write drive currents while writing or a forward coupling bias to the read sense lines during reading. The bias arrangement is shown in Figure 5-3.

Transistors Q9 and Q10 form a single-input differential amplifier. When either transistor is turned on, the other is turned off. Transistor Q9 is turned on during a read operation, and Q10 is turned on during a write operation.

During a write operation, Q10 is turned on by the low-active Write Enable Right Matrix (WRENA RM/) signal. With Q10 on, the positive voltage level at the intersection of diodes CR59 and CR60 pulls current from the −24-volt source through R57 and CR59 and through R58 and CR60. This current back-biases diodes CR56 and CR58, effectively disabling the read preamps. Diodes CR31 and CR32 are also back-biased by the negative voltage at this time. Write current flows through diodes CR11 and CR12 (Figure 5-2).

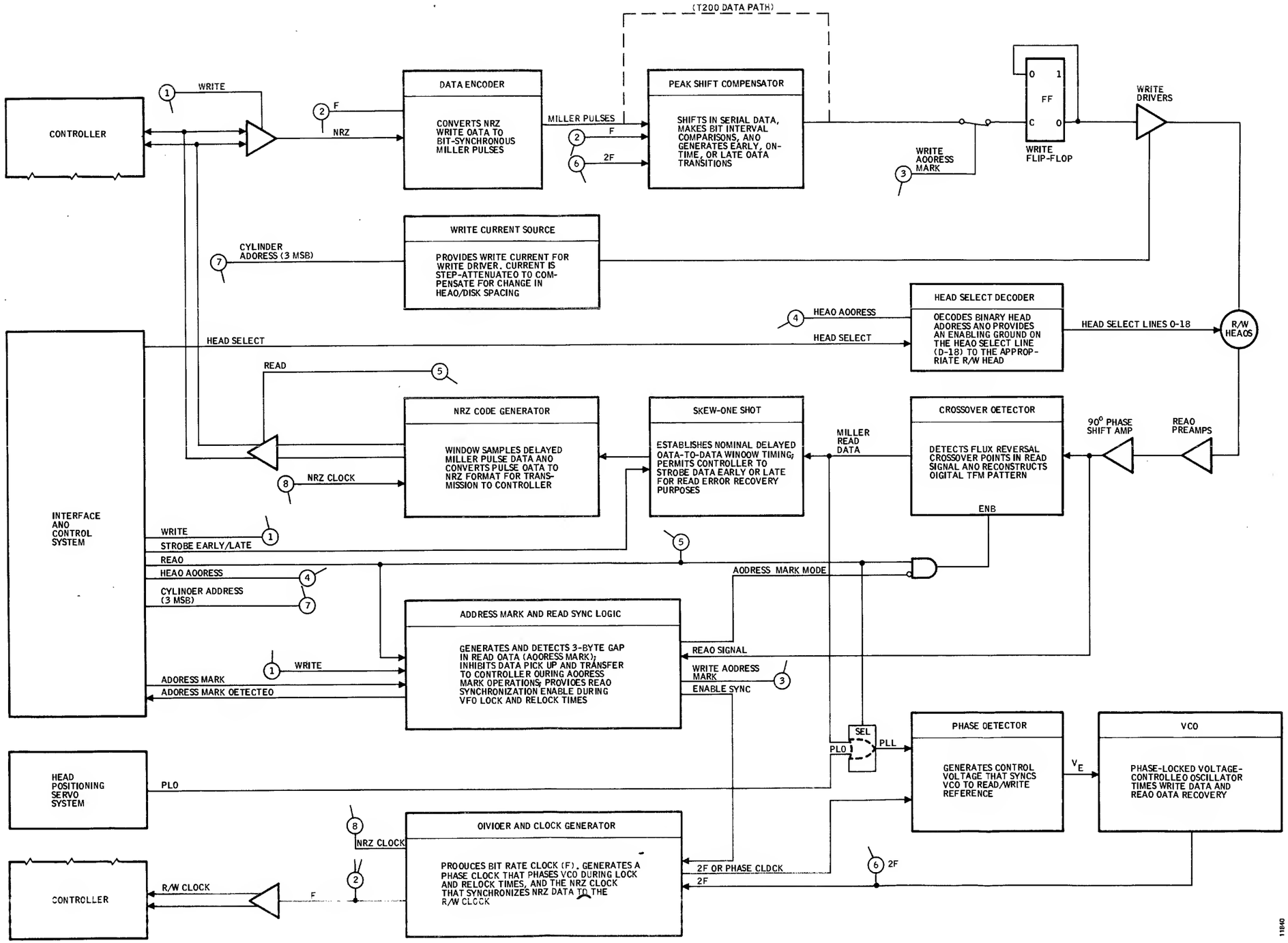

Figure 5-1. Read/Write System, Block Diagram

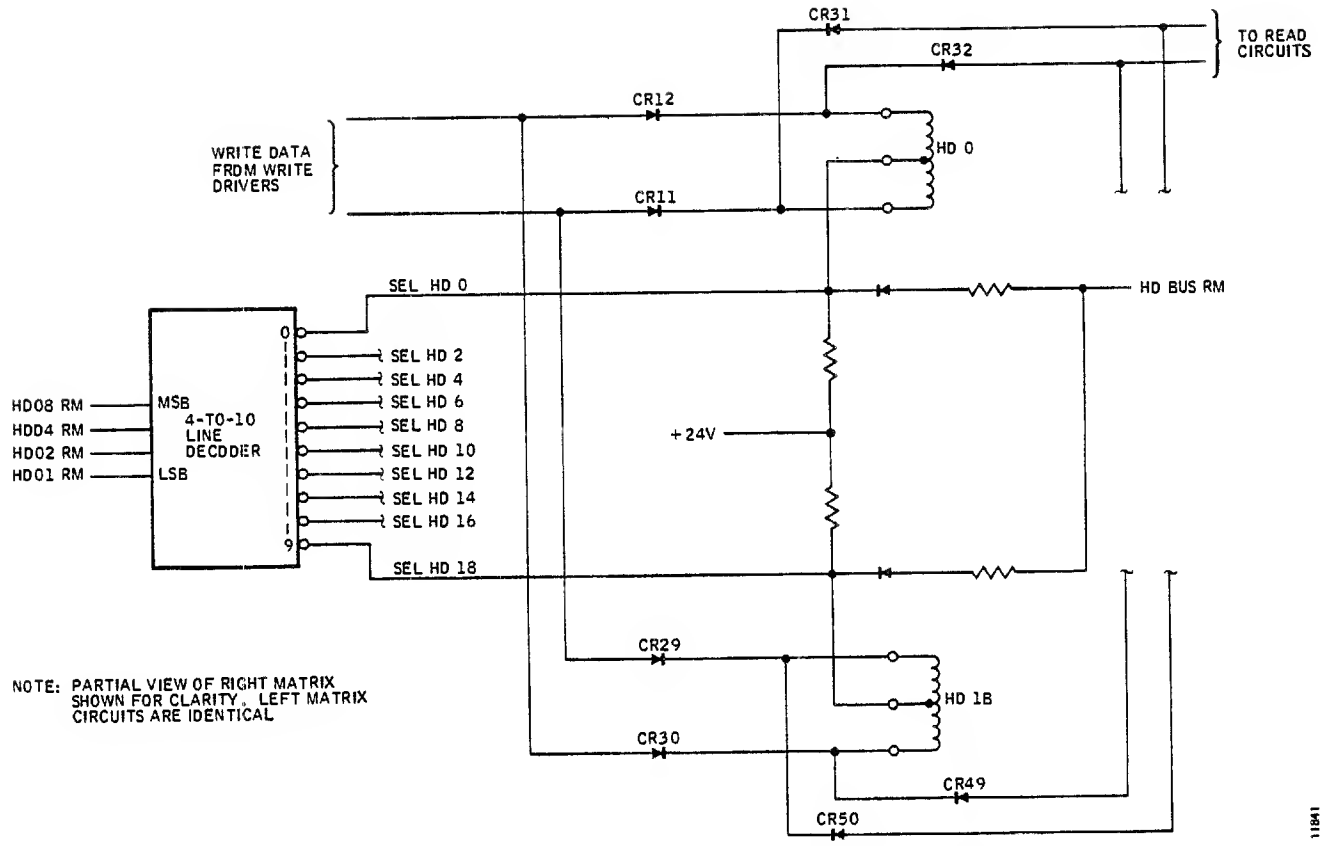

Figure 5-2. Head Select and Read/Write Matrix, Simplified

At the conclusion of a write operation, WRENA RM/ goes high, which causes Q10 to turn off. The fast-rising positive voltage pulse at the emitter of Q10 appears at the emitter of Q9 and causes that transistor to turn on and remain on. Diodes CR31 and CR32 are forward-biased by the current through resistor R55, and diodes CR56 and CR58 are forward-biased by the current flowing through them. Diodes CR54 and CR55 establish clamp levels for the read signals. Differential read data is developed across resistors R57 and R58, and this data is sent to the read preamps for amplification.

Details of the write data current control and read data signal processing are discussed in detail later in this section of the manual.

HEADS SAFE/UNSAFE DETECTION

The read/write heads are monitored for activity to ensure that one and only one head on each matrix board is selected at all times. Each head-select center-tap line is connected to either the HDBUS LM or HDBUS RM line (as appropriate) through separate resistors and coupling diodes. See Figure 5-2. If a head is not selected, the +24-volt pullup voltage back-biases the decoupling diode; this causes the unselected head to be decoupled from the bus line. The safe/unsafe detection scheme is based on the fact that one head on each matrix board is always selected, and the current through each of the monitoring circuits is essentially the same.

It was mentioned earlier that there were 19 active heads (heads 0-18) and a single dummy head. Since the left matrix contains only nine active head matrix circuits while the right matrix contains 10, the decimal 9 output of the decoder on the left matrix is connected to the dummy head. Remember that the HAR logic provides active HD01LM and HD08LM addresses when the head-select line is down. This arrangement ensures that one and only one head on each matrix board is selected at all times.

The Heads Unsafe Detection Logic is shown in Figure 5-4. Each Head Bus (HDBUS) line feeds a sense amplifier that monitors the current flowing in that line. As long as one head is connected on each line, the ORed comparator remains high. The circuit detects two conditions:

- More than one head connected on either line
- No head connected on either line

Should either of the above conditions occur, a low output will be provided from one comparator or the other, causing the Heads Unsafe Signal (HDUSF/) to go active. When head switching occurs, HDUSF/ will drop temporarily (a *glitch* appears on the line) but the

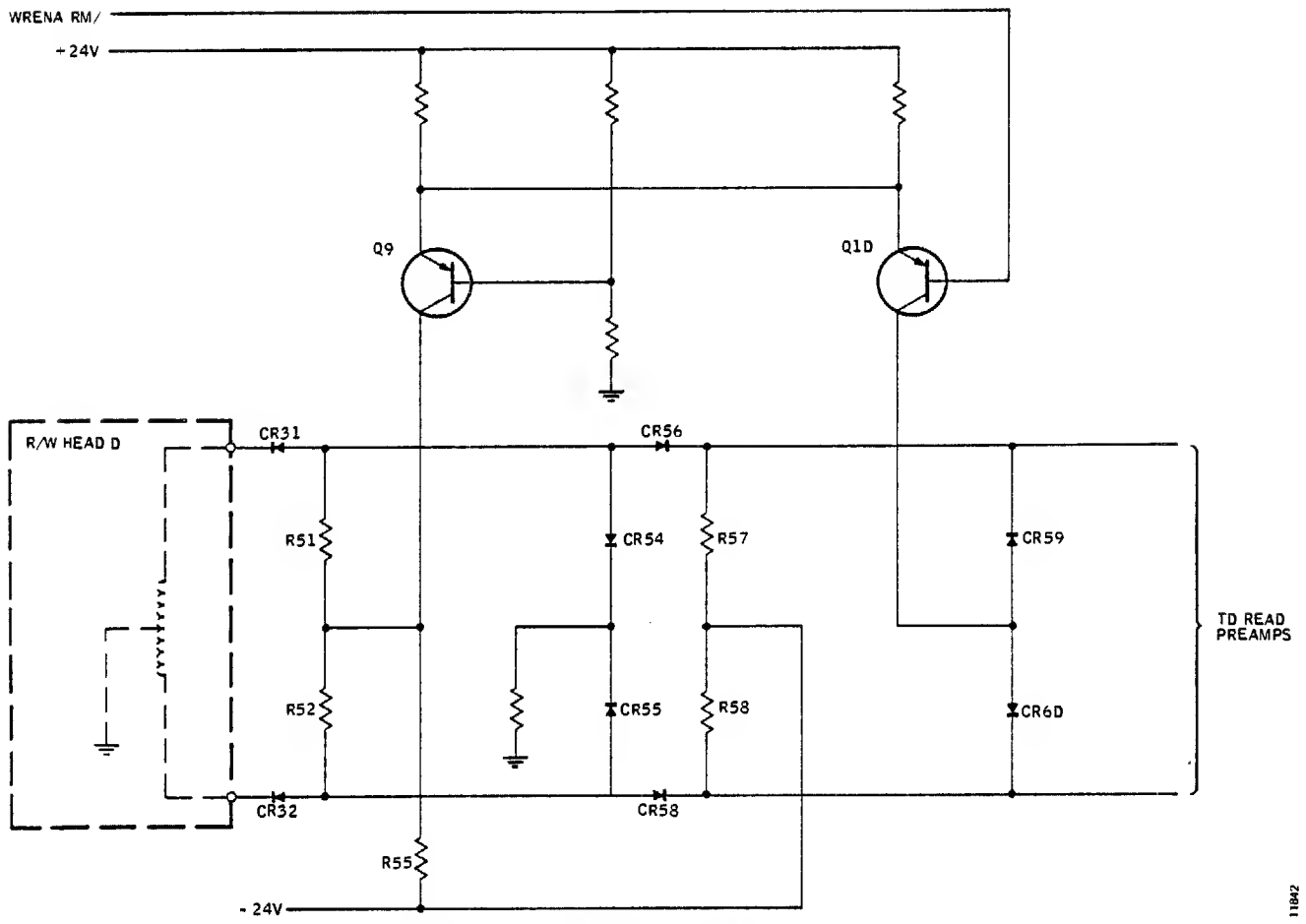

Figure 5-3. R/W Matrix Biasing Arrangement

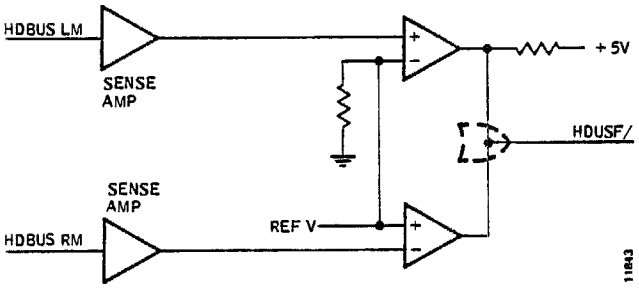

Figure 5-4. Heads Unsafe Detection Logic, Simplified

error detection logic differentiates between this normal temporary condition and an actual error condition; the latter-mentioned condition generates a device-check condition. This operation is described in the Status and Error Detection section of the manual.

ADDRESS MARK AND READ SYNC LOGIC

The Address Mark and Read Sync Logic is shown in Figure 5-5. Address marks are required when a variable-length sector format is used. Synchronization for the read circuits is provided by this logic regardless of whether or not address marks are used. In addition to the analog circuit that monitors the read

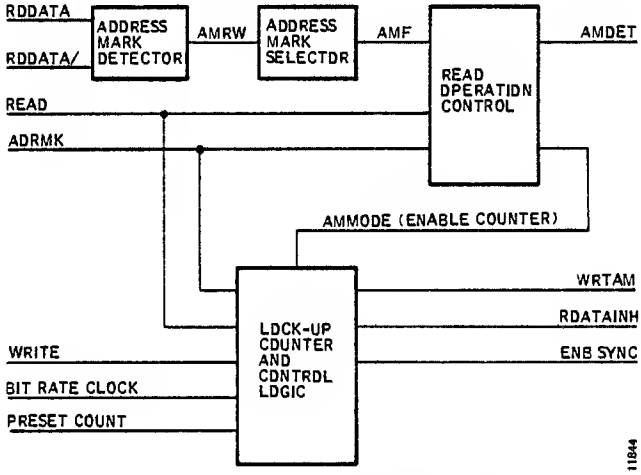

Figure 5-5. Address Mark and Read Sync Logic, Block Diagram

signal, the following four digital logic circuits are used:

- An Address Mark Detector
- An Address Mark Selector
- The Lock-Up Counter and Control Logic
- A Read Operation Control Circuit

The Address Mark Detector is basically an analog circuit although it uses a hybrid output comparator. This circuit monitors the differential read data lines for signal activity and detects a loss of signal transitions. The Address Mark Read/Write (AMRW) signal is generated when this occurs, and the Address Mark Selector begins a timing cycle to ensure that the loss of transitions is the result of an address mark and not a bad spot on the disk.

After the timing cycle is complete, the selector provides an input to the Read Operation Control indicating that an address mark has been found (AMF). The Read Operation Control then issues Address Mark Detected (AMDET) to the controller and enables the Lock-Up Counter and Control logic with the Address Mark Mode (AMMODE) output.

When the Lock-Up Counter and Control Logic is enabled, it initiates an automatic load and begins a 48-bit (T300) or 26-bit (T200) count. During the count time, it provides the following outputs:

- WRTAM — inhibits write data from write drivers
- RDATAINH — inhibits read data from being sent to the controller
- ENBSYNC — provides an enable signal that enhances the correct clock phasing operation for the VFO oscillator during VFO lock and relock time

The key to understanding the operation of the subject logic during a read operation is the state of AMMODE signal. This signal controls the start of a timing cycle only when an address mark format is used. If address marks are not used, AMMODE performs no function; the timing cycle begins as soon as READ becomes active. When address marks are used, AMMODE does not become active until the detection circuits have verified the presence of the recorded address mark. This event starts the timing cycle previously referred to.

When a Write Address Mark operation is programmed, the ADRMK and WRITE signals initiate a 24-bit time count. The WRTAM signal inhibits write data for this 3-byte period, thereby creating the address mark. Since the ADRMK signal is inactive in systems that do not use address marks, the address mark logic performs no function during write operations in those systems.

Address Mark Detection

The circuits that detect the 3-byte address mark are shown in simplified form in Figure 5-6. Address mark monitoring is performed by the analog circuits shown in the upper half of the diagram; the digital control and timing logic that ensures that an address mark has been detected is shown in the lower half of the diagram.

Differential inputs for the Address Mark Detection circuits are picked off the input to the Crossover Detector and Digitizer. The attenuating resistors in the input legs isolate and prevent interaction between the circuits. A differential amplifier brings the attenuated signal back up to a usable level.

A full-wave rectifier applies a pulsating dc waveform to the Level Translators. The Level Translators are nonlinear amplifiers; they provide very low amplification for low-level inputs and very high amplification for higher-level signals, and thereby improve the signal-to-noise ratio of the circuit.

Pulsating dc from the translators is smoothed by a filter circuit. A characteristic of this filter is to dump an accumulated charge quickly. This provides for a negative-going pulse with a fairly rapid fall time when the heads enter the Address Mark area and the transitions cease.

It should be noted that the sine wave shown at the input to the differential amplifier occurs during an all-zero preamble. Significant differences appear at other times; however, these changes do not affect the detection operation.

A combination Linear Amplifier/Digital Comparator converts the analog input to digital logic levels. One characteristic worthy of note is that there is no phase inversion between the inputs and outputs of the element. Unless the head is reading an address mark, the input to the circuit is positive, and the differential outputs allow a high output to the digitizer and a low output to the Sync and Counter Direction Flip-Flop.

When the head enters the address mark area, the input level drops until the data transitions reappear. With the low input and the Address Mark Mode (AMMODE) signal high, the enable/disable output to the digitizer is driven low to disable that circuit, and the Address Mark Read/Write (AMRW) signal goes high. Unless an address mark is being read, RDGATE controls the enable/disable line to the digitizer; the comparator output level is not sufficient to enable the line otherwise.

The control and timing logic comprises the Sync and Counter Direction Flip-Flop, a nine-bit up-down counter, a Count Sense Flip-Flop, and the Start/Stop Control Logic.

The controller commands the address mark search by transmitting the READ and ADRMK signals over the bused interface to the drive. When this occurs, the Start/Stop Control Logic generates AMMODE and conditions the counter for a count mode. In addition to the functions described previously, AMMODE enables the PLO signal to clock the Sync and Counter Direction Control flip-flop.

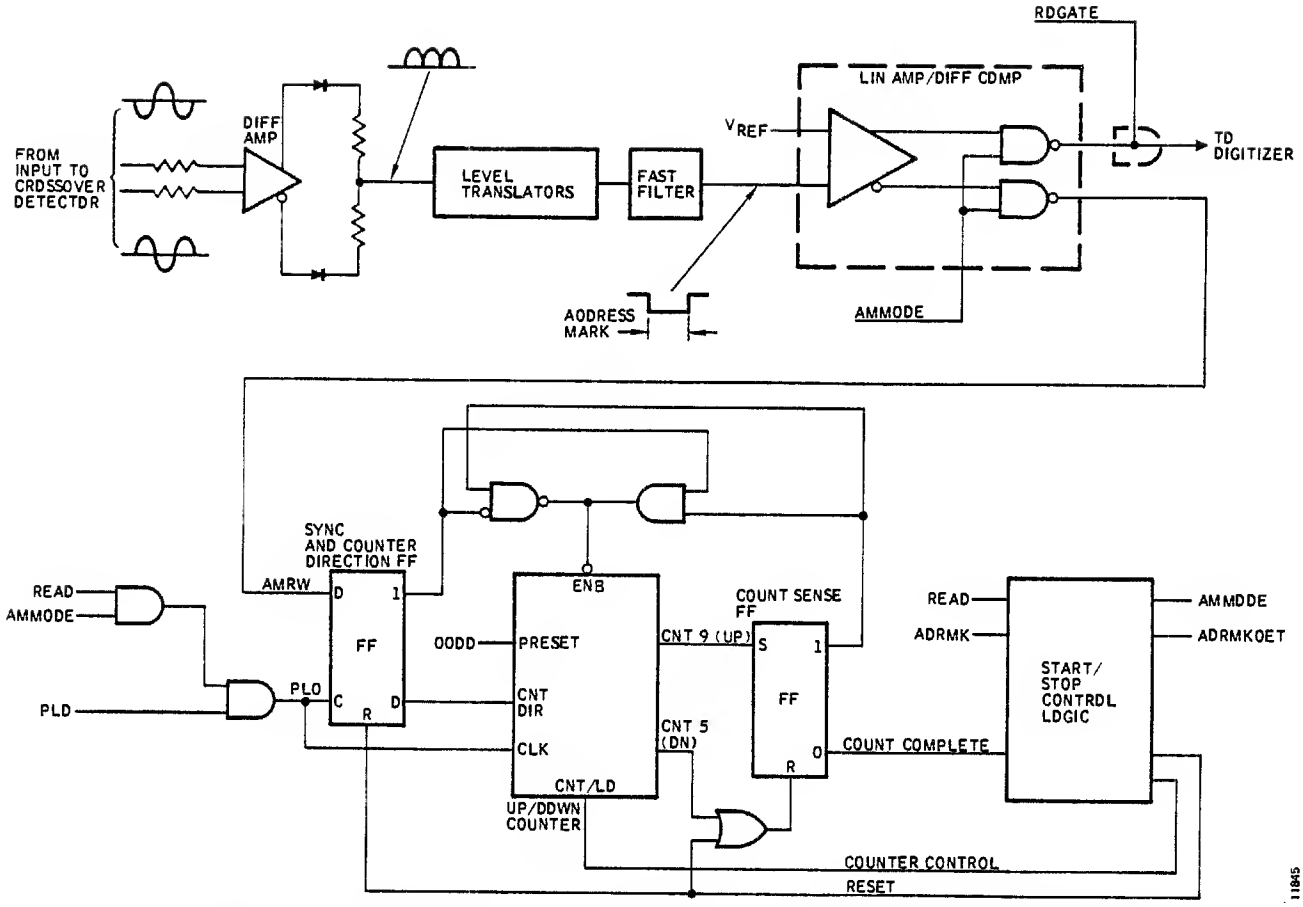

Figure 5-6. Address Mark Detection and Operation Control Circuits, Simplified

When the Address Mark is detected, AMRW goes high (see Figure 5-7); the resulting low input to the counter initiates an up-count operation. The count continues through count 9; at which time, the Count Sense flip-flop is set, thereby disabling the counter. An advantage of this circuit is that it can differentiate between a bad spot on the disk and an actual address mark. A bad spot can cause a false count to begin; however, the bad spot will be of short duration and the control and timing logic will sense the fall of AMRW before the up count is terminated. A down count is then initiated automatically and the logic waits for AMRW to go high again and initiate another up count.

As the Address Mark area moves out from under the heads, AMRW falls and the counter is enabled for a down count. When the down count reaches 5, the Count Sense FF is reset and it signals the Start/Stop Control Logic that the full count sequence has been completed. The counter is then reloaded, the Address Mark Detected (AMDET) signal is generated, and the circuit is reset for the next detection operation.

WRITE DATA CONVERSION

Write data is received in NRZ form from the controller over differential read/write data lines and routed to the Data Separator card. The NRZ data is converted to Miller code and enabled to either the right or left matrix at this point. Since the data conversion circuits are not the same for the T200 and T300, they will be described separately in the following paragraphs.

Write Data Code Conversion Logic (T200)

The Write Data Code Conversion Logic for the Model T200 is shown in Figure 5-8. NRZ data is enabled through the line receiver by the WRITE command (not shown) and then applied to the Auto Phase Select and Sync Detector.

During a write operation, the disk drive transmits the bit-rate clock (F) signal that is in sync with the disk drive PLO servo signal to the controller. This allows the controller to send synchronized NRZ write data to the drive. However, because of the time delay inherent in the connecting cables, the data must be resynchronized at the drive. The Auto Phase Select and Sync Detector samples the NRZ data at twice the bit frequency (2F) and produces a synchronized NRZ output.

Synchronized NRZ data is directed to a two-bit shift register that holds the current and previous bits of the

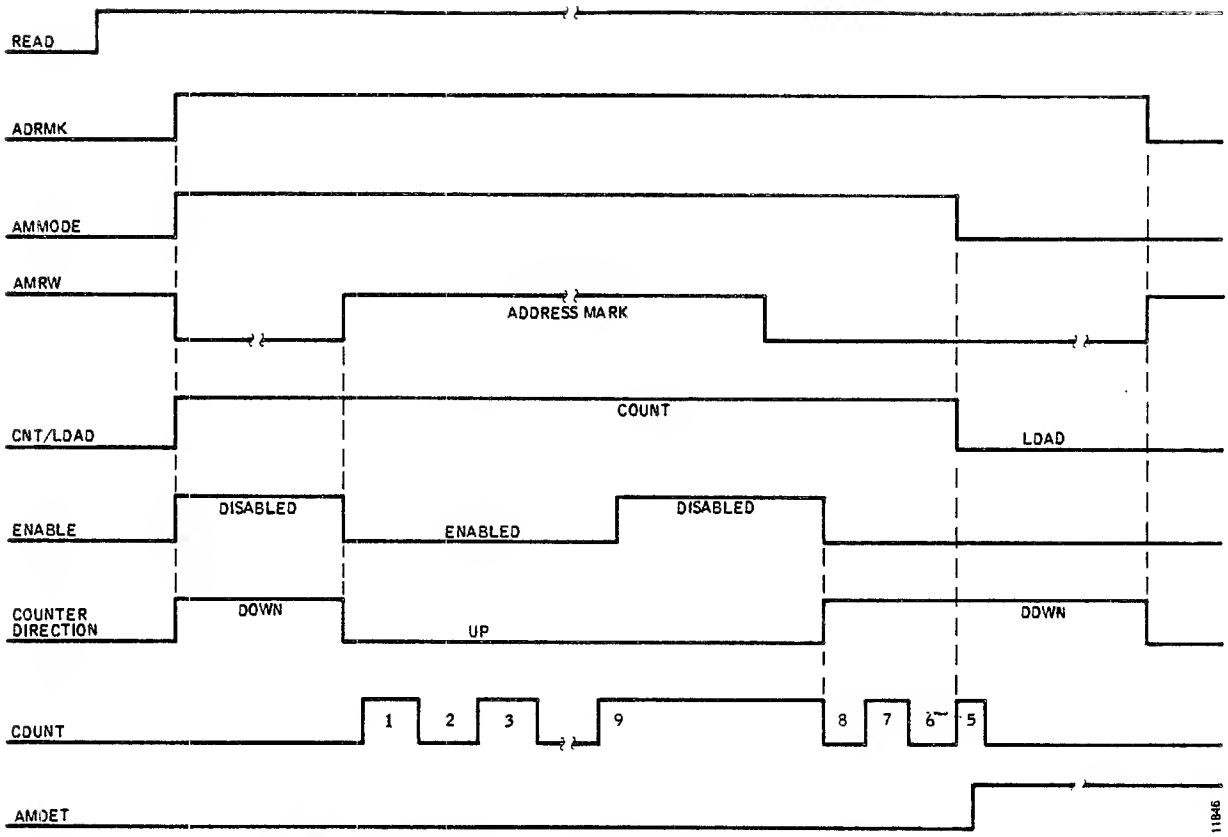

Figure 5-7. Address Mark Detection Timing Diagram

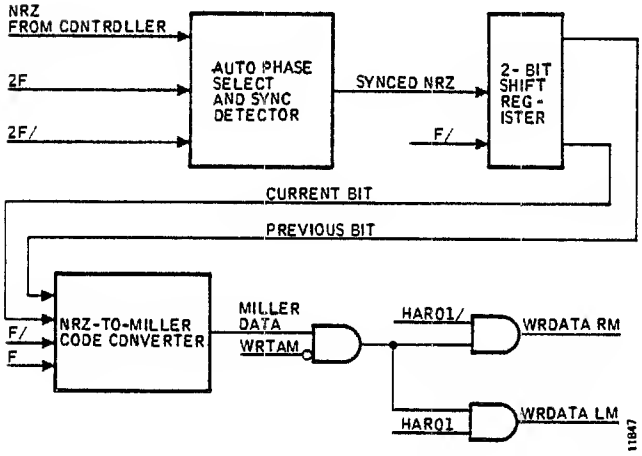

Figure 5-8. Write Data Code Coversion Logic (T200), Simplified

data train. The NRZ-to-Miller Code Converter combines these two bits with the F and F/ clock signals to develop the Miller-coded data. The least-significant bit in the HAR gates the data out to the previously-selected head matrix.

During a write address mark operation WRTAM inhibits the output from the code converter to create the three-byte address mark of no transitions.

Write Data Code Conversion Logic (T300)

The Write Data Code Conversion and Compensation Logic for the Model T300 is shown in Figure 5-9. This logic differs from the conversion logic in the Model T200 drive in that it incorporates peak-shift compensation for the higher write frequencies encountered in the T300.

NRZ data is enabled through the line receiver by the WRITE command (not shown) and then applied to the Auto Phase Select and Sync Detector.

During a write operation, the disk drive transmits the bit-rate clock (F) signal that is in sync with the disk drive PLO servo signal to the controller. This allows the controller to send synchronized NRZ write data to the drive. However, because of the time delay inherent in the connecting cables, the data must be resynchronized at the drive. The Auto Phase Select and Sync Detector samples the NRZ data at twice the bit frequency (2F) and produces a synchronized NRZ output.

Synchronized NRZ data is directed to a five-bit shift register that holds the current bit, two previous bits, and two future bits of the data train. The NRZ-to-Miller Code Converter combines the two previous bits with the F and F/ clock signals to develop the Miller-coded data.

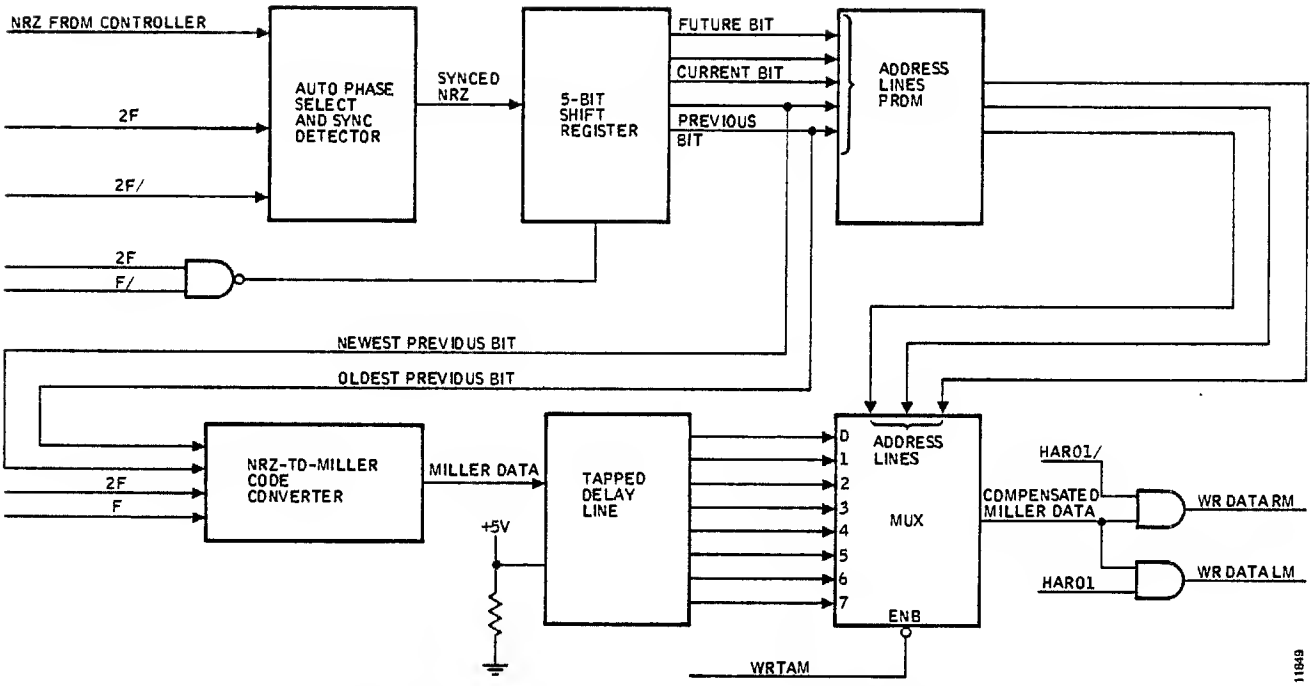

Figure 5-9. Write Data Code Conversion and Comparison Logic (T300), Simplified

As mentioned previously, peak shift occurs at the high write frequencies used in Trident T300 disk drives. The peak-shift compensation circuit that determines whether to write a bit transition early, on time, or late analyzes the pattern in the five-bit shift register to make the determination.

The five-bit pattern in the shift register is used as an address for a PROM that contains the correct write time for all possible data patterns. These write times are actually three-line, binary addresses.

Miller pulses from the code converter travel through the Tapped Delay Line that provides eight different delayed outputs. One of these outputs is selected for each pulse by the three-line, binary address output of the PROM that is applied to the MUX. The least-significant bit in the HAR gates the Compensated Miller Data from the MUX to the previously selected head matrix.

During a write address mark operation, WRTAM disables the MUX output to create the three-byte address mark of no transitions.

WRITE DRIVE LOGIC

The write drive logic converts the Miller code pulses from the write compensation logic to TFM code write transitions that control the on/off state of the write drivers. Since the right-hand matrix board contains two circuits not found on the left-hand board, it is noted in the logic illustrated in Figure 5-10. The following functional circuits are a part of the write drive logic:

- Write Flip-Flop
- Current Drivers
- Write Current Compensator
- 24-volt Regulator
- Write Unsafe Switch

The Write Data Right Matrix (WRDATARM) signal that clocks the write flip-flop is actually the compensated Miller Data from the write compensation logic. See Figure 5-9. This data is available to the write drive logic during online operation when the drive is not degated and a write operation is programmed. It should be noted that the exerciser can also generate write data when the drive is offline.

The write flip-flop is always held disabled by the false state of WRENARM except during a write operation. During a write operation, the leading edge of each WRDATARM pulse clocks the flip-flop, causing it to toggle. Each output of the flip-flop controls a current driver; the drivers alternately switch current to the inputs of a differential amplifier that produces the current for the read/write heads.

The two circuits that are unique to the right-hand matrix are the +24v Switch and the −24v Regulator. The switch disables the +24VS line should an unsafe condition occur, thereby disabling the current drivers. The regulator provides a very precise current to the current drivers. In this circuit, the minus voltage controls the actual output of the current driver.

Write Error Detection

Both the write transitions and the write current are monitored by error-checking logic. During a write

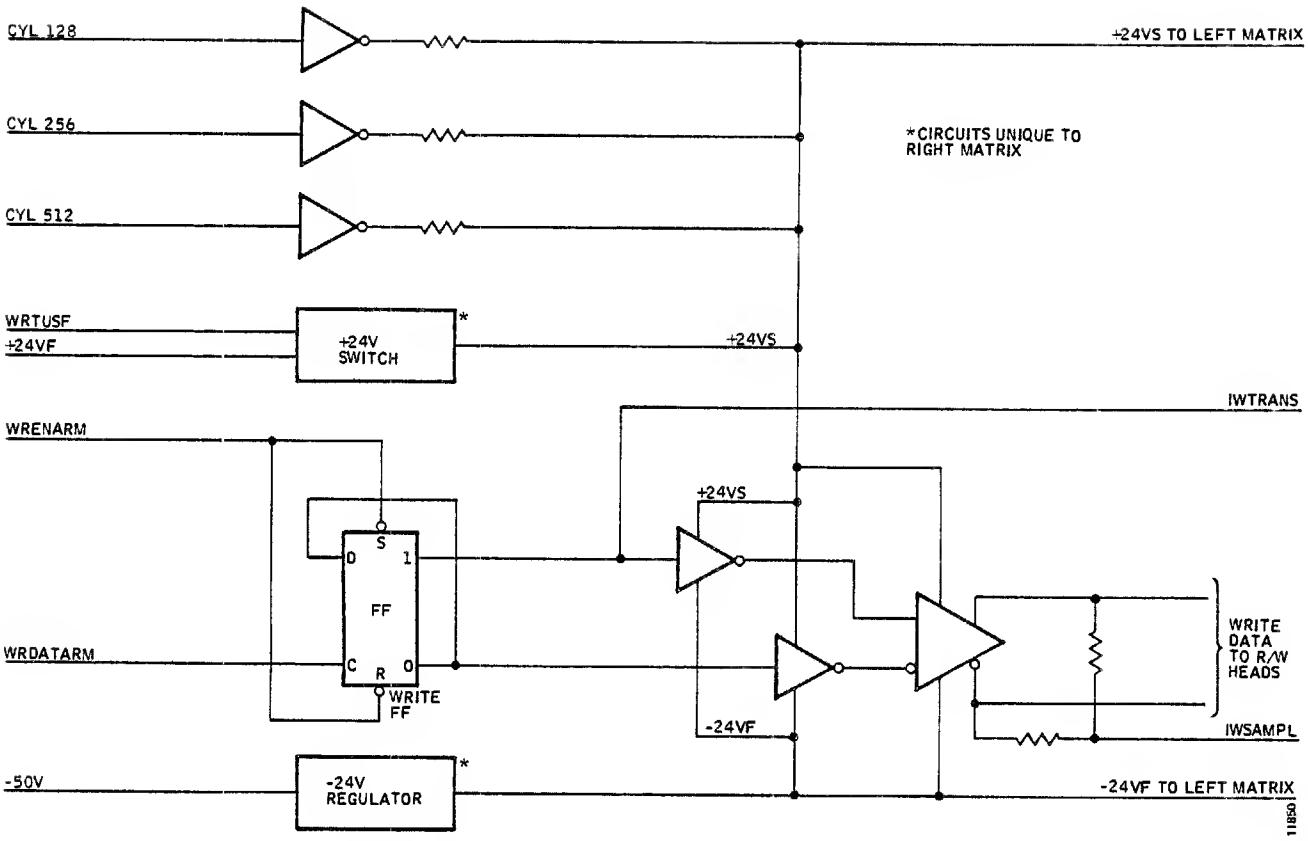

Figure 5-10. Write Drive Logic, Simplified

operation, write current transitions (IWTRANS) must occur within a specified time frame; otherwise, the write unsafe (WRTUSF) signal goes active and removes the +24VS supply from the write drivers to inhibit the write operation and initiates a device check. The monitor circuit that performs this function is described in the Status and Error Detection Section of the manual.

Two comparators (Figure 5-11) monitor the activity of the write drivers by sampling the write current (IWSAMPL RM and IWSAMPL LM) from each read/write matrix and comparing it to a reference voltage. The circuit detects the following conditions:

- Whether or not the write driver is turned on at the correct time

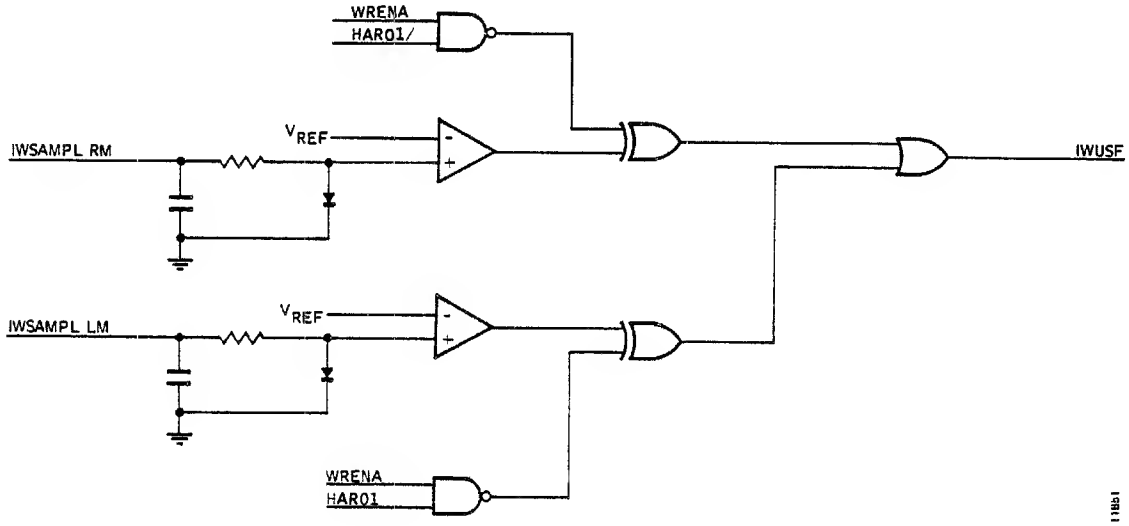

Figure 5-11. Write Current Unsafe Detection Logic, Simplified

- A defective head winding
- A head that is unplugged or otherwise unable to receive head enabling or write current
- Too much or too little write current

Basically, the comparator provides an output appropriate to the operation in progress and the current sample. During a normal write operation, the output levels of the active and passive comparators match the output levels of their associated gates. If this is not the case, the Write Current Unsafe (IWUSF) signal becomes active and initiates a device check. The manner in which the device check is initiated is explained in the Status and Error section of the manual.

The Write Drive timing diagram (Figure 5-12) shows a sampling of signals derived from the Miller code pulse train and the effects these signals have on write current transitions. Please note that, for clarity, the timing relations between MILLER, EARLY, ON TIME, and LATE are not accurate. All peak-shift compensation delays have been lumped together and are reflected in the shifting of the WRDATA signal position.

The electrical and aerodynamic characteristics of the read/write heads largely determine the magnitude of write current employed. Table 5-1 shows typical values for disk drive heads. As mentioned earlier, the write current is reduced in six incremental steps from its maximum value as the head is positioned closer to the disk spindle to compensate for a reduction in head flying altitude and increased bit density as the head moves inward. Without this stepping down of the write current, track flux saturation would occur, reducing frequency response and increasing the probability of crosstalk between tracks.

TABLE 5-1. WRITE CURRENT CHARACTERISTICS

Write Current Zone	Track Address Range	T200 and T300 Write Current (ma. p-p)
1	000-127	106.7 ±5.5
2	128-255	103.3 ±5.5
3	256-383	100.0 ±5.5
4	384-511	96.7 ±5.5
5	512-639	93.3 ±5.5
6	640.767	90.0 ±5.5
7	768-814	86.7 ±5.5

READ SIGNAL PROCESSING

Analog signals detected by the heads during read-mode biasing of the Read/Write Matrix boards are coupled to a grounded-base amplifier (Figure 5-13) that constitutes the first stage of the matrix board preamplifier. For purposes of simplicity, only the details of the Left Matrix board are shown on the drawing; the Right Matrix is electrically identical.

Outputs of the grounded-base input amplifier (Q12 and Q13) are directed to the second preamplifier

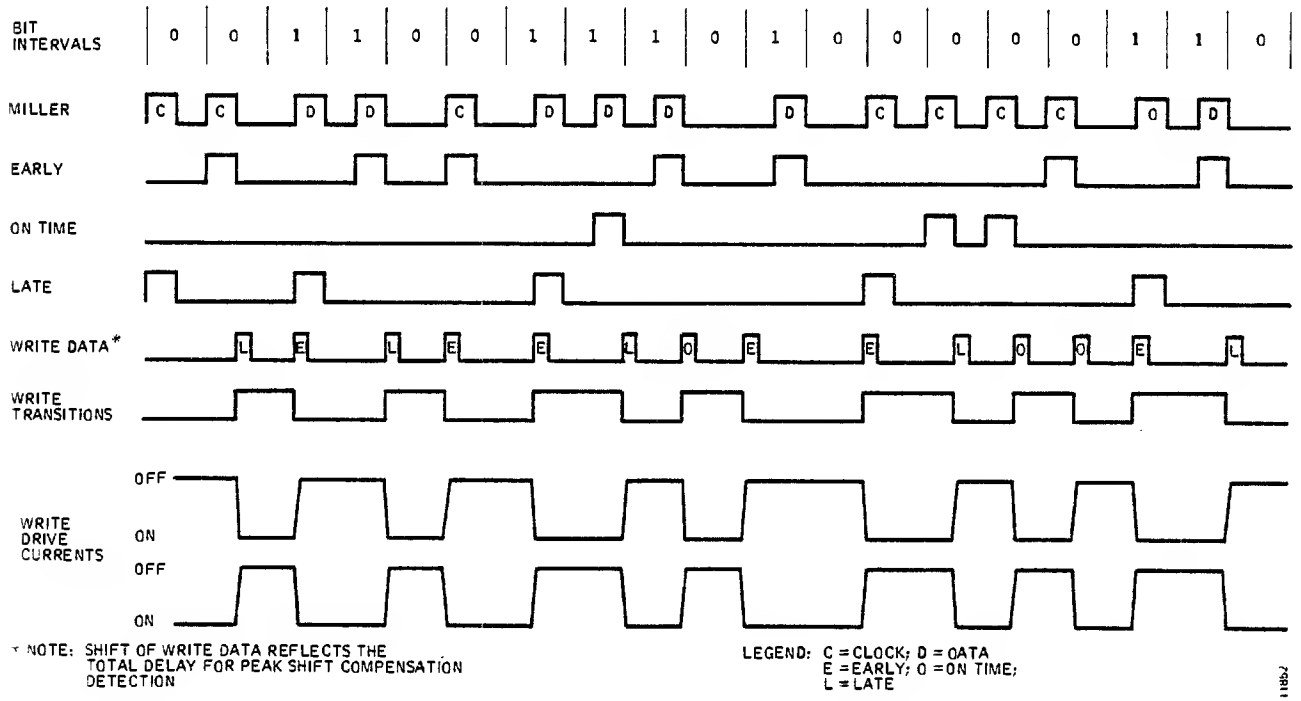

Figure 5-12. Write Drive Timing Diagram

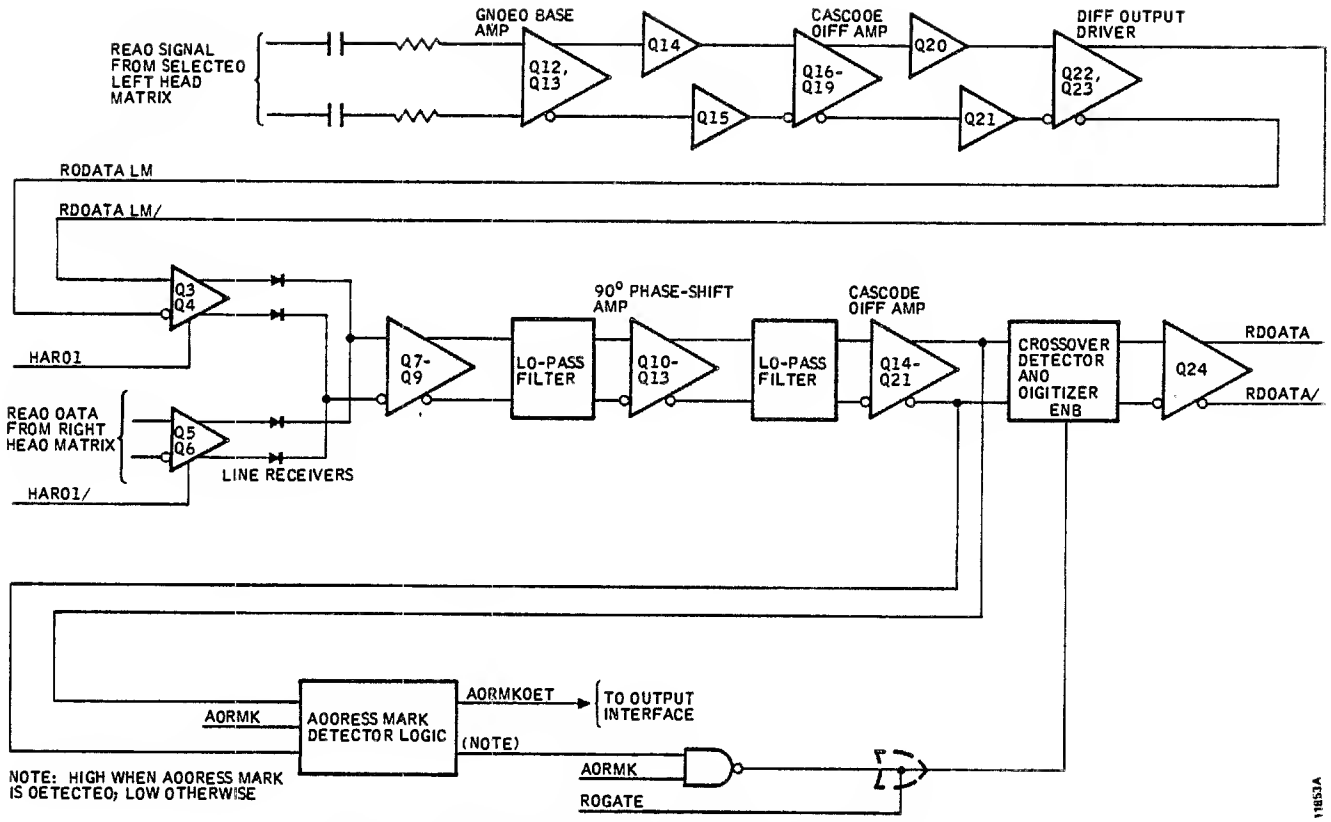

Figure 5-13. Read Signal Processing Circuits, Simplified

stage, Q16 thru Q19. These elements comprise a cascode differential amplifier, chosen because of its high-gain, low-noise characteristics. Emitter followers Q14, Q15, Q20, and Q21 provide buffering between the preamp stages.

Matrix board differential outputs RDDATALM and RDDATALM/ are sent to the Read Limiter card through differential Input Line Receivers Q3 thru Q9. Two low-pass filter networks reject most spurious components of the read signal, but primarily they filter out the higher-order harmonic components of the three base frequencies of the signal.

A 90-Degree Phase Shift Amplifier (Q10-Q13) is interposed between the two filter networks. The function of this amplifier is to simplify the job of detecting the edges of read pulses. Recall that at the instant of flux reversal in the record, a maximum read signal amplitude will be produced by the head. If a threshold level detector were to be used to digitize the analog signal, the actual moment of transition would be signal-amplitude and rise-time dependent and also subject to erroneous triggering by noise spikes. By differentiating the signal 90 degrees lagging, the recorded flux transition now occurs at the point of minimum signal amplitude or zero volt. This crossover point is much less ambiguous in time, is less subject to spurious error pickup, and is easier to detect with precision.

Another high-gain, cascode differential amplifier (Q14 thru Q21) produces a very high level signal that has a steep rate of change slope through the zero crossover points of the signal. This final analog output is presented to the crossover Detector and Digitizer circuits for conversion to Miller code pulses. These circuits will be discussed shortly in detail.

The Address Mark Detector Logic monitors the differential read data signal for activity during an address mark search. Generation and detection of address marks is covered under the Address Mark and Read Sync Logic heading in this section and only the general function of the logic during read mode will be mentioned here.

When the controller transmits a read address mark (ADRMK) command, the subject logic begins monitoring the read data lines. As the selected head enters the address mark area, the logic is delayed a short time to ensure that the head is really in an address mark area, then initiates a timing cycle. When the timing cycle is started, the Address Mark Detected (ADRMKDET) signal is transmitted to the controller and the Crossover Detector and Digitizer circuits are inhibited. The last mentioned circuits are enabled by RDGATE except during address mark detection.

CROSSOVER DETECTION AND DIGITIZING

The analog read-data signal comes from the last signal amplifier as a differential pair with data transitions timed to the zero-crossover points. These crossover points are detected by applying the signal to the inputs of a combination linear amplifier/differential comparator. (Figure 5-14). This comparator works like a squaring amplifier by changing output states each time the differential input signals reverse polarity at the zero-volt crossover points.

The squared differential outputs are applied to a logic network that comprises two one-shots, an OR gate, a time delay circuit, and a flip-flop. This network is commonly referred to as the *desnake* circuit. The read head suffers from decay between flux transitions, particularly at the lower frequencies encountered while reading on the outer (lower-numbered) cylinder positions. These *snakes* are shown in waveform ① of Figure 5-15 where the false crossovers occur in the center of a flux transition. Their effect appears in the output of the squaring amp, as in waveform ②. The *desnake* circuit makes the digitizer insensitive to these false crossovers by delayed sampling of the squared output of the comparator.

Both outputs of the comparator are directed through identical one-shots to an OR gate so that either leading edge of a transition generates a narrow pulse output from the OR gate. One output of the comparator is applied directly to the delay flip-flop set input so that the flip-flop will be enabled before the clock pulse occurs. Delayed and nondelayed clock signals are shown in waveforms ③ and ④ of Figure 5-15. By delaying the clock pulse train (waveform ④) beyond the point of false zero-crossover activity (approximately 40 percent of a bit time), the output of the delay flip-flop (waveform ⑤) does not reflect any false crossovers.

READ/WRITE CLOCK GENERATION

The Data Separator board contains the Voltage-Controller Oscillator and frequency divider that generates the bit rate synchronous clocks for write data timing and for establishing the windows for read data recovery. The Read/Write Clock supplied to the drive interface for controller synchronization is also produced by this oscillator.

Synchronism of the Voltage-Controlled Oscillator is established by phase-locking the oscillator output to incoming RDDATA pulses during Read mode operation and to the PLO output when not in Read mode as long as the heads are loaded. Figure 5-16 shows the VCO and its synchronizing circuits in simplified form.

The free-run (heads unloaded) center frequency of the VCO in T200 drives is adjusted to 12.90 megahertz. or twice the bit rate frequency of 6.45 megahertz. The VCO in a T300 drive has a center frequency of 19.35 megahertz, which is also twice the 9.68 megahertz bit rate frequency. This free-running oscillator frequency

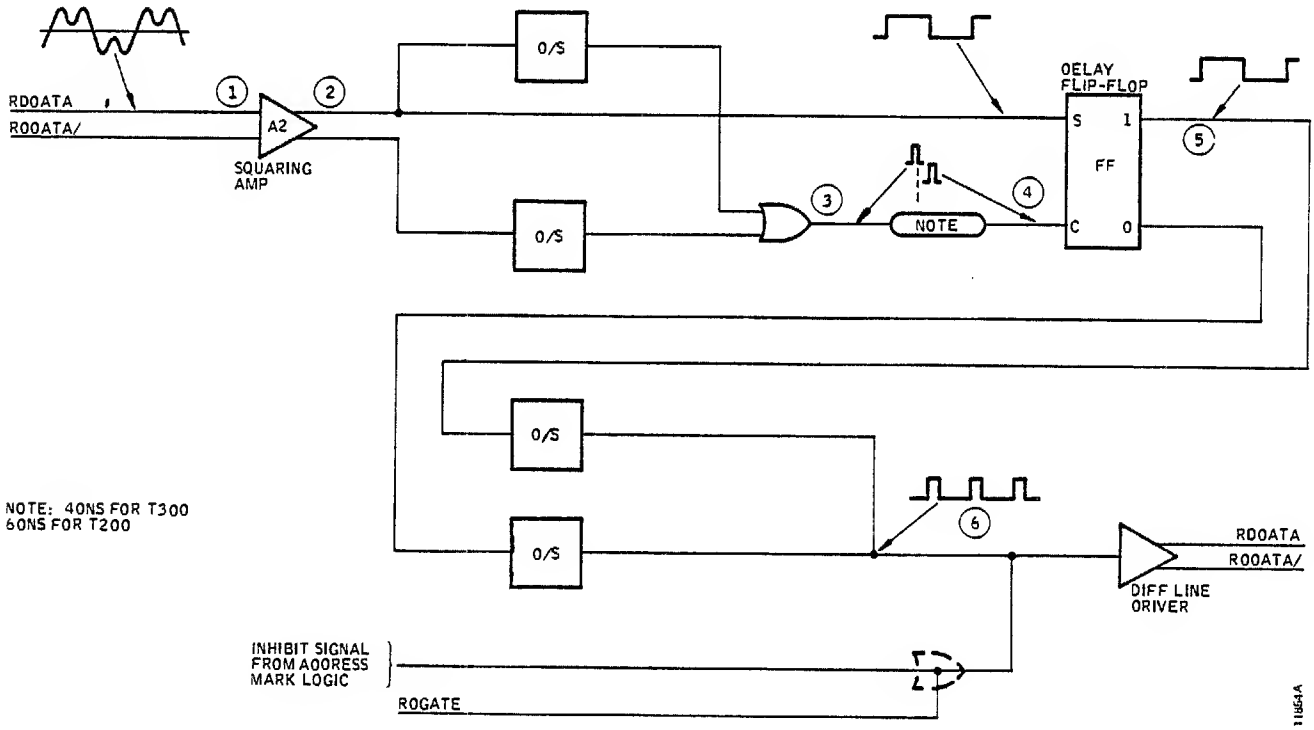

Figure 5-14. Crossover Detector and Digizer Logic, Simplified

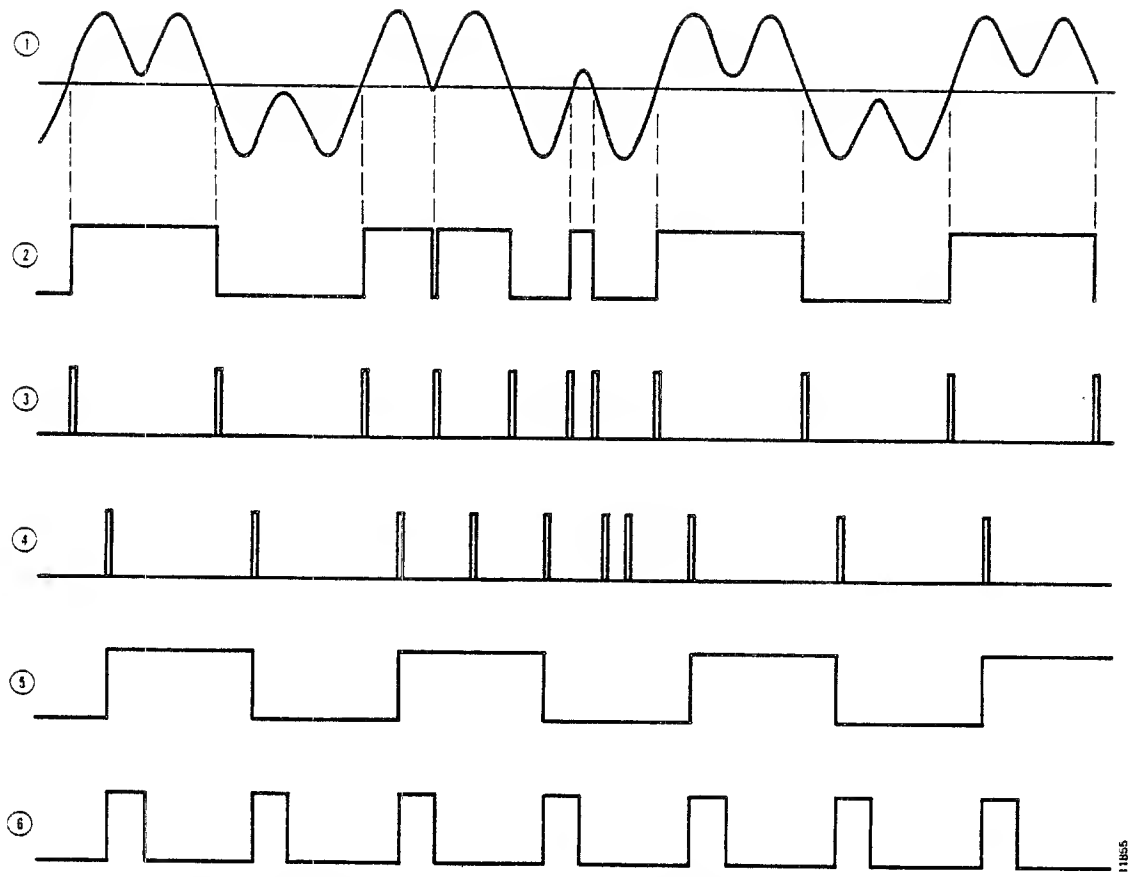

Figure 5-15. Crossover Detector and Digitizer Timing Diagram

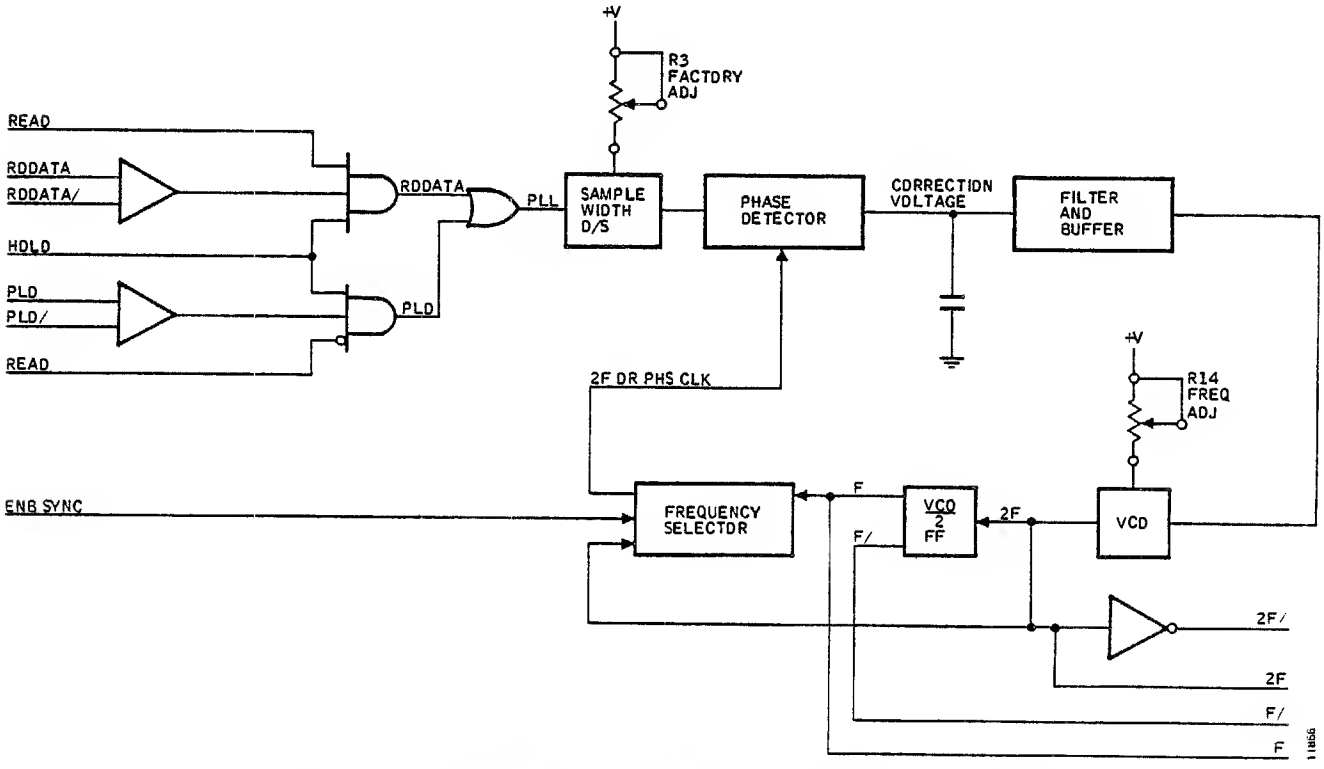

Figure 5-16. Phase Lock Loop Voltage-Controlled Oscillator, Simplified

is set by varying the frequency adjustment of the VCO, and the center frequency is established by the input level to the VCO. Positive or negative swings from a predetermined level will slow down or speed up the oscillator, respectively.

Control of the VCO is determined by the phase relationship between the Sample Width One-Shot output and the VCO output frequency. The Sample Width One-Shot determines when the phase comparison will be made, the length of time during which it will be made, and whether or not any comparison will be made at all. The latter statement obviously requires clarification. When the data pattern is 101, there is no data pulse during the 0 time.

The phase detector is disabled by the one-shot during the 0 data time to prevent an invalid comparison, so it functions as a sample-and-hold device during this particular event. At all other times, it provides the reference signal for VCO correction. It is adjusted at the factory for optimum performance by the setting of potentiometer R3; *adjustment should not be attempted in the field.*

The phase detector looks at the one-shot and VCO outputs and provides a pulse output (correction required) or no output (no correction required). The width of the pulse determines the magnitude of the correction voltage stored by the integrating capacitor. A Filter and Buffer circuit refines the correction voltage and isolates the integrating capacitor and the VCO.

Center frequency for the VCO is established when the input voltage level is a nominal 2.7 volts. The output of the VCO is adjusted for optimum performance with FREQ ADJ potentiometer R14.

A flip-flop divider develops the bit rate frequency (F) from the 2F VCO output. The F and 2F signals and their respective complements are supplied to other read/write circuits for timing purposes.

READ SYNCHRONIZATION

In an earlier discussion involving the Address Mark and Read Sync Logic, mention was made in passing that synchronization of the read circuits was initiated by the action of the Lock-Up Counter (see Figure 5-5) that is a functional part of that logic.

What actually happens is that the ENBSYNC output of the counter modifies the operation of the feedback circuit to the VCO (see Figure 5-16) to enable it to shift phase very rapidly. The VCO frequency remains unchanged during the VFO lock and relock operations; only the phase changes.

One other point that should be stressed again is that synchronization of the read data is independent of whether or not address marks are used in track formatting. The synchronization process is essentially the same, regardless of the chosen track format.

During a read operation, the VCO oscillator must be synchronized with a known reference before any of the playback data is meaningful. In the Trident format scheme, an all-zeros field always precedes the data. This all-zeros field is the known reference that allows the read drive circuits to differentiate between a one and a zero. While the all-zeros field is being read, the VCO is phase-locked to the playback data so that the data and clock signals that are later transmitted to the controller are correctly phased.

During VFO lock and relock periods that precede the transfer of meaningful data to the controller, it is desirable to sync the VCO to the read data in the shortest possible time. Phase-locked loops (PLL) normally compensate for slow frequency and phase variation caused by changes in disk speed. From drive to drive, this change can approach ±5 percent.

By following slow variations, a PLL predicts (from a time average of a previous cell) the beginning and end of a data bit cell. Some modification of circuit response is therefore desirable to speed up the lock-up time.

The above-mentioned circuit modification is achieved by combining the ENBSYNC signal in the Frequency Selector Gate Logic with both the F and 2F clock signals to produce a special clock signal (PHSCLK) (Figure 5-16) that enhances the ability of the phase detector to respond very quickly to phase differences, and thereby speed up the lock-up time of the entire PLL. Since this condition is not desirable except during read sync lock and relock periods, it is used only during these times. During all other times, the 2F clock signal is compared with the PLL input to establish phase difference and corresponding voltage level inputs to the VCO.

Read synchronization timing is shown in Figures 5-17 and 5-18. When a format involving address marks is used an all-zeros field is written immediately following the address mark. This field is commonly referred to as the VFO lock time. Notice that the lock-up counter begins counting down during the address mark time and counts out before the beginning of the sync field. It is during this count time that the ENBSYNC output of the counter enables the VCO to lock up to the data as it is read from the disk. When the counter counts out, data is enabled out to the controller, which is looking for the all-ones sync byte that ensures that the following data is valid.

DATA DETECTION AND NRZ CODE GENERATION

The incoming PLL signal not only provides the reference for phase-locking the VCO output frequency, but

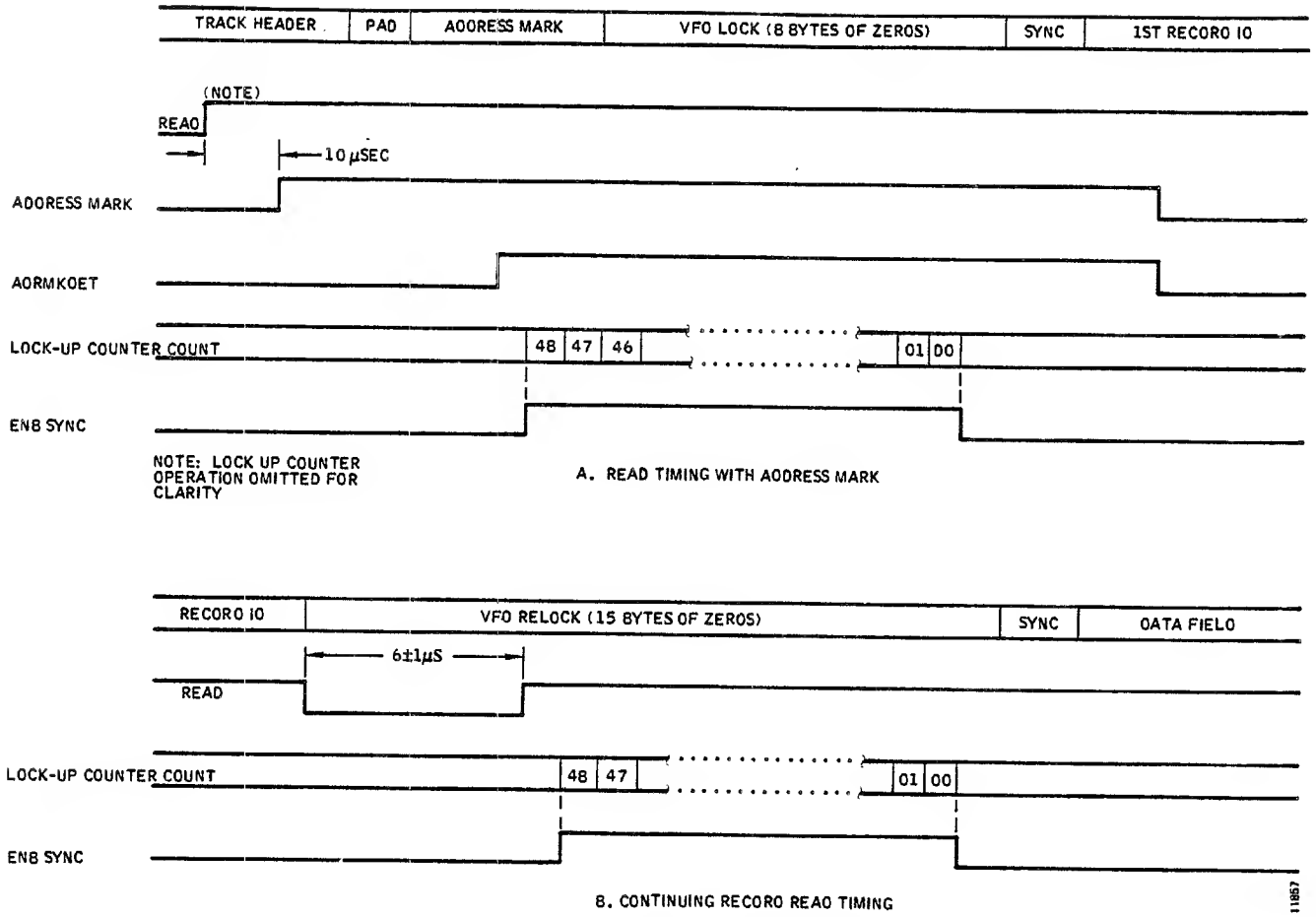

Figure 5-17. Read Synchronization Timing Diagram (T300)

it also serves as the clock signal that generates the detected data pulse.

In Section 1 of this manual, reference was made to setting up accurate strobe windows relative to the raw data being read. This statement was appropriate at that time because of the general nature of the discussion; however, it was an oversimplification. In actuality, the strobe window and the read data are the same signal at the drive interface. The method of developing this signal is discussed in the following paragraphs.

During a read operation the PLL signal (Figure 5-19) is read data unless an address mark search is in progress. Notice that AMMODE enables PLO while inhibiting RDDATA; however. AMMODE is dropped once the address mark is detected, and the PLL signal is read data during the VFO lock and relock times shown in Figures 5-17 and 5-18.

The PLL signal picked up from the disk is passed through a factory optimized delay line before it clocks the Window Skew One-Shot. A rising input edge to the one-shot produces a negative-going pulse. The rising edge of the skew one-shot output is Exclusive-ORed with the STROBE EARLY and STROBE LATE commands from the controller and the resulting output, as well as the aforementioned commands, is applied to the timing gates. A certain amount of delay is inherent in the gate circuit; the STROBE EARLY command will cause less delay than the absence of either of the strobe commands (STROBE ON TIME), which in turn will cause less delay than the STROBE LATE command.

When the rising edge of the STROBE pulse occurs, it triggers the Window Width One-Shot which in turn produces the Detected Data Pulse. See Figure 5-20. Notice in the timing diagram that the Data Pulse occupies the center half of the bit cell when it is correctly adjusted.

The NRZ Clock Generator provides a composite clock signal derived from the F and 2F clocks. This NRZ clock edge-triggers the NRZ Code Generator at the approximate center of the bit cell time. Observe that the cycle time of the NRZ clock is equal to the bit rate frequency, F. This arrangement provides the correct phasing for the NRZ data and Read/Write Clocks, also shown on Figure 5-20.

NRZ data is supplied to the controller when READ is active and RDATAINH (inhibit signal produced

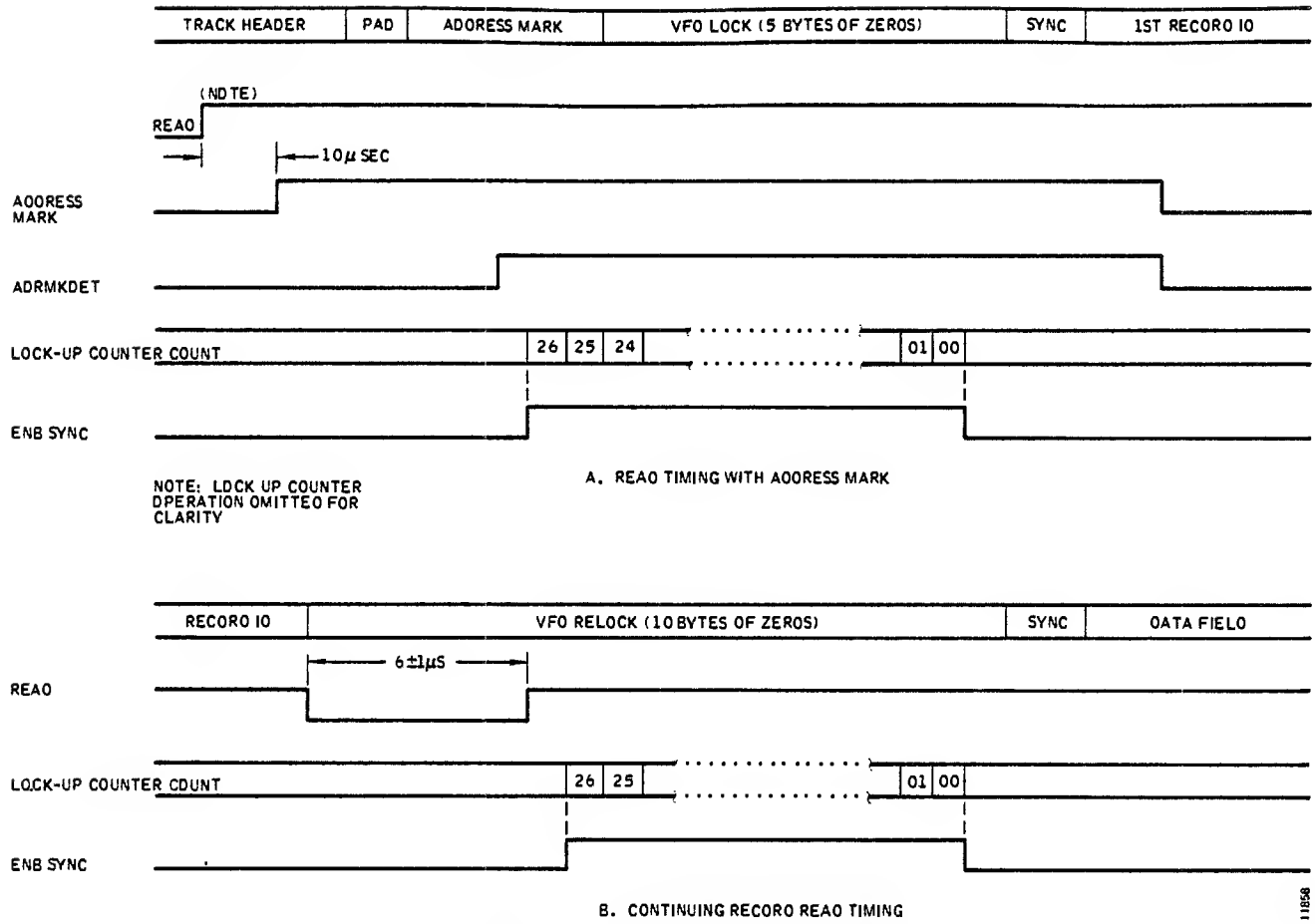

Figure 5-18. Read Synchronization Timing Diagram (T200)

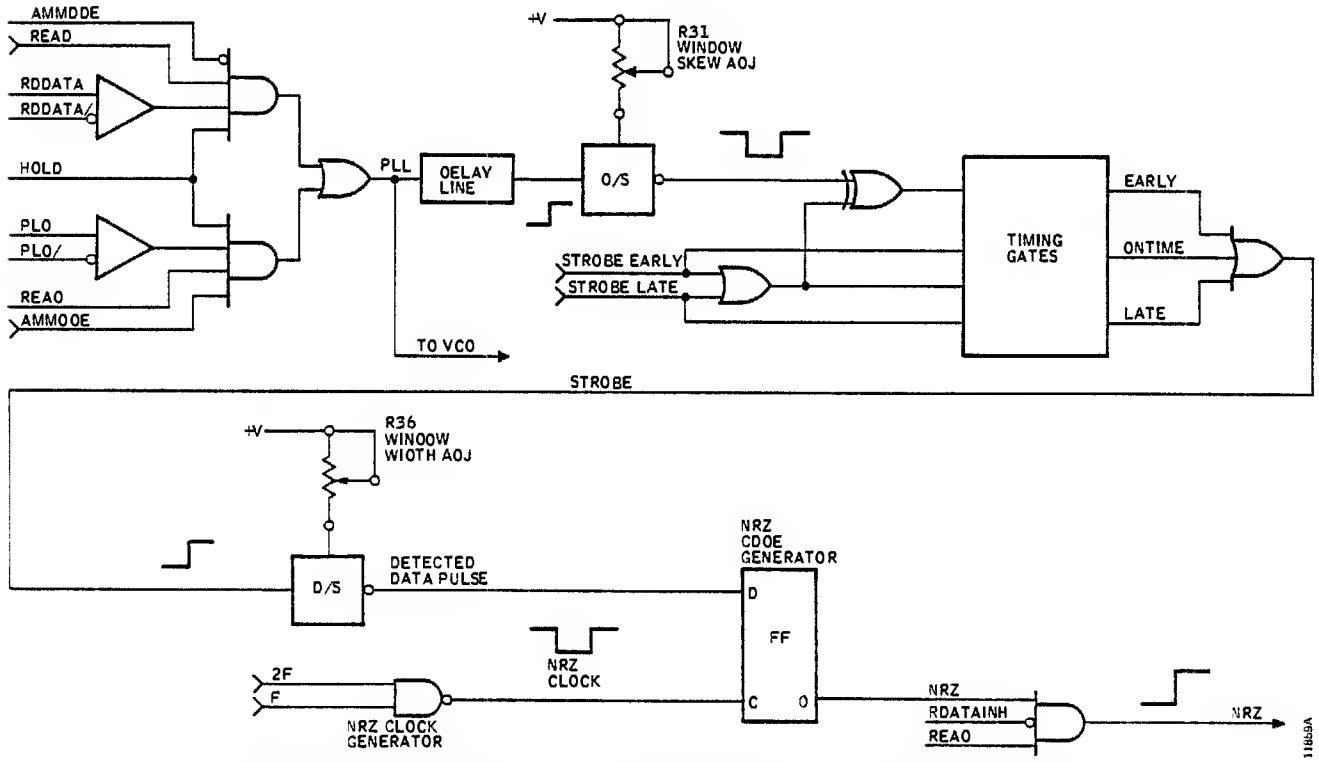

Figure 5-19. Data Detection and NRZ Code Generator Logic, Simplified

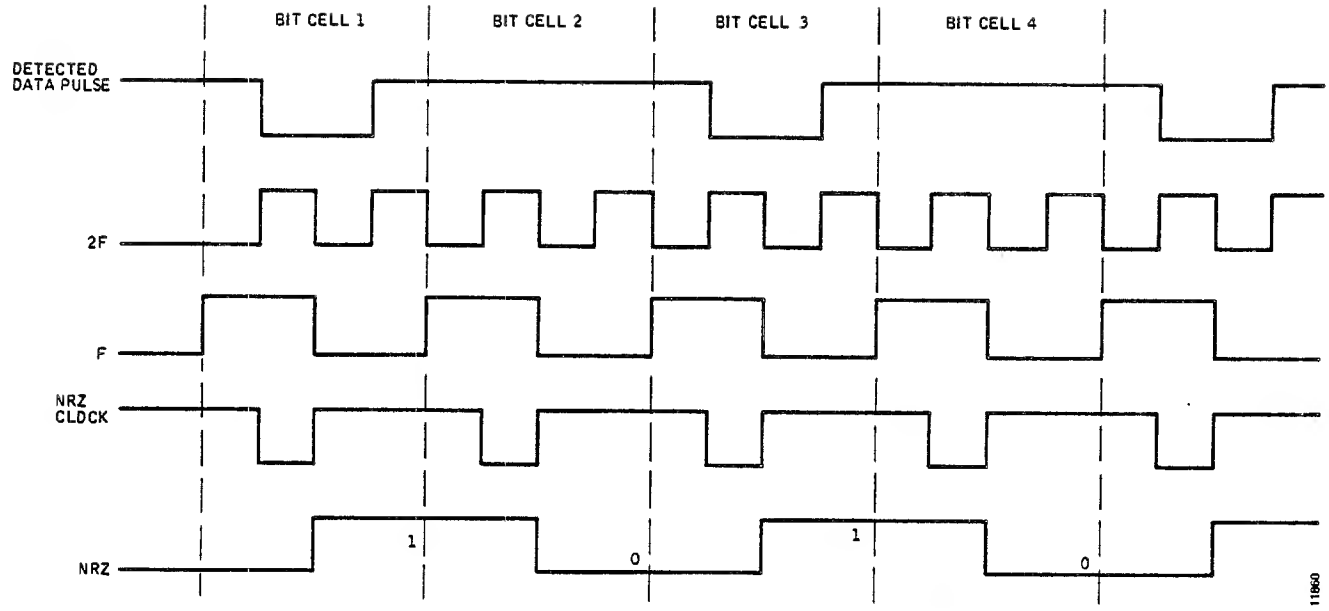

Figure 5-20. Data Detection and NRZ Code Logic Timing Diagram

during VFO lock and relock times) is inactive. The Read/Write clock at the F (bit rate) frequency is also transmitted with the read data for synchronization purposes within the controller.

READ-ONLY INTERLOCK LOGIC

The setting of the READ ONLY — READ/WRITE switch on the operator control panel determines whether the machine will perform read-only (file protect) or both read and write operations. In either case, it is imperative to prevent inadvertant operation of the switch from affecting an operation in progress.

Figure 5-21 illustrates the Read-Only Interlock Logic. Notice that the Interlock Gates *lock in* the switch setting when the drive is selected. The logical state of the switch can be changed during a rezero operation while the drive is selected, but this is the exception to the rule. Normally, switch changes are made when the drive is deselected.

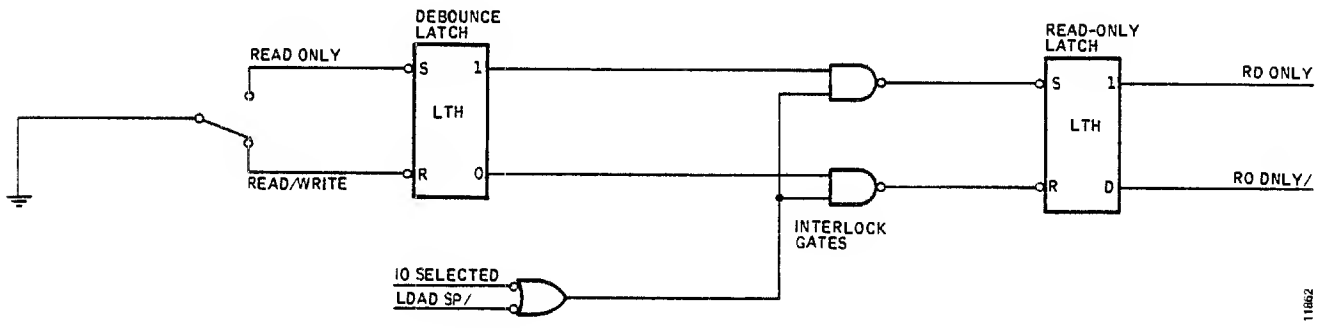

Figure 5-21. Read-Only Interlock Logic

SECTION 6
STATUS AND ERROR DETECTION

This system consists of the Attention (Interrupt) Logic, Device Check Logic, and Status Drivers that return disk drive status signals to the controller. Figure 6-1. shows the components of this system.

When the disk drive is online (Interface/Degate switch is not active), status on the Attention and Composite Sector/Index lines is available to the controller at all times. All other status lines require the drive to be selected by the controller. These signals and the drive systems that provide them are shown in Figure 6-1.

ATTENTION INTERRUPT LOGIC

The Attention line functions as an interrupt and becomes active when any one of the following conditions is detected:

- Seek has been completed
- Seek start is commanded with a difference count of zero
- Seek is not completed within approximately 0.9 second
- An Emergency Retract has occurred

The attention logic (Figure 6-2) varies slightly for single- and dual-access machines. Both types use the single Attention Flip-Flop, and dual-access machines require two flip-flops in addition to the Attention Flip-Flop.

Attention is activated at the completion of any seek operation by the Ready signal. A no-motion seek start occurs when a seek command is issued with a count of zero in the difference counter. This is a normal operation for some controllers and is usually done for purposes of software expediency. The drive responds to this common by simply raising ATTN.

Abnormal conditions such as seek incomplete or emergency retract operations also generate Attention signals.

The controller can distinguish the seek-incomplete interrupt from the seek-completed interrupt by monitoring the disk drive status lines. The SKINC line will be active and will remain active until the controller issues a rezero command to generate Attention Reset (ATTN*R). The interrupt may also be reset by issuing the normal Read command.

Any emergency retract sets the Attention flip-flop to activate the Attention interrupt line. The emergency retract condition is signalled to the controller by the abrupt dropping of online status when the heads are retracted. The usual controller response to attempt recovery from an emergency retract is to sequence power down and back up. If this fails, operator intervention is required. The interrupt is cleared by such intervention or by a Read command.

In the dual-access environment, the Attention signal for either access (AATTN, BATTN) is developed after the selection process has been completed and the access has been connected (A CONNECTED, B CONNECTED).

DEVICE-CHECK FAULT LOGIC

Device Checks are fault conditions that would result in unsafe operation if not detected. A Device Check inhibits the initiating operation from being executed and prevents further operations from being executed until the Device Check is rest by a direct command from the controller. Device Check conditions include:

- Setting a cylinder address while the drive is not ready
- Setting an offset while the drive is not ready
- Receiving an illegal cylinder address (greater than 814)
- Initiating a seek while offset is active
- Writing while the drive is not ready
- Writing off track center
- Writing when READ ONLY switch is active
- Writing while offset is active
- No write transitions for 40 microseconds while writing
- Write current is unsafe
- No head or more than one head is selected during reading or writing (heads unsafe)

All device check errors except seek when not ready, seek while offset, and illegal cylinder address can be reset by a Device Check Reset command from the controller. The exceptions require a rezero operation for reset.

Figure 6-3 shows the logic that detects and stores conditions that initiate a Device Check.

During a write operation, the write transitions are monitored by a 3-microsecond one-shot while they are being recorded. If a predetermined number of bits are dropped consecutively, a DATAFAULT will be generated. This signal may or may not be meaningful; DATAFAULT must remain active for 45 microseconds before a read/write unsafe (RWUSF) signal is generated.

The RWUSF flip-flop monitors write transitions, write current, and the number of heads selected. For example, if the write current source rises above or falls below unsafe levels (IWRUSF active) or no head (or more than one head) is actively selected (HDUSF active), the D-input of the flip-flop will be gated high and a 45-microsecond delay one-shot will be triggered to supply the setting clock. This delay in the clock reduces the sensitivity of the logic to transient error conditions.

When RWUSF becomes active, it not only initiates a Device Check, but is also generates the Write Unsafe (WRTUSF) signal that turns off the current to the write driver circuits. An emergency retract operation performs the same function. Notice that only a Device Check Reset (DEVCHK*R) signal from the controller can reset the RWUSF Flip-Flop.

Two other conditions that initiate a device check should be noted at this time. One is an attempted seek to an illegal cylinder, and the other is an attempted seek while offset. Notice that both conditions set a latch that can only be reset by LOADSP during a first seek repower-up or a rezero operation.

When the Device Check latch is set, the clock signal (LTHCLK) that normally rides high falls, thereby locking the error condition that caused the Device Check into one of the CE convenience latches. As long as power is not removed from the drive, the latch retains the error information. Observe that the DEVCHK Flip-Flop can be cleared by DEVCHK*R only if the latch that directly sets the DEVCHK Flip-Flop is not set. If that latch is set, a first seek repower-up or a rezero operation is required to clear the Device Check condition.

STATUS DRIVE LOGIC

The status drive logic varies depending upon whether or not the dual-access option is incorporated in the machine. In single-access machines, three status signals are returned to the controller via the radial cable, and the remaining ten are returned over the bused cable that is common to all drives in the system. See Figure 6-4. An additional signal is added to the radial cable when the dual-access option is employed. See Figure 6-5.

Notice in both figures that all 13 single-access or 14 dual-access line drivers require an enabling signal; this signal is the DEGATE signal, and it is supplied only when the Interface/Degate switch is in the ONLINE position. Low level true outputs are provided by all drivers. Signals carried by the radial cable are ungated while those carried by the bused cable are transmitted only when the drive is selected. The radial cable for dual-access units contains one output status signal not found in single-access units. This is the Request From Other Controller (AREQFMB or BREQFMA) signal. It is provided for those systems that require this information for decision making within the controller(s) or software).

When either access is disconnected as a result of a simultaneous attempt by both controllers to capture the access, all line drivers are disabled except the one associated with the Composite Sector/Index (COMPSECiDX) signal. This signal is unaffected when the access is not connected and the dual-access is operating in automatic mode, regardless of which access is connected.

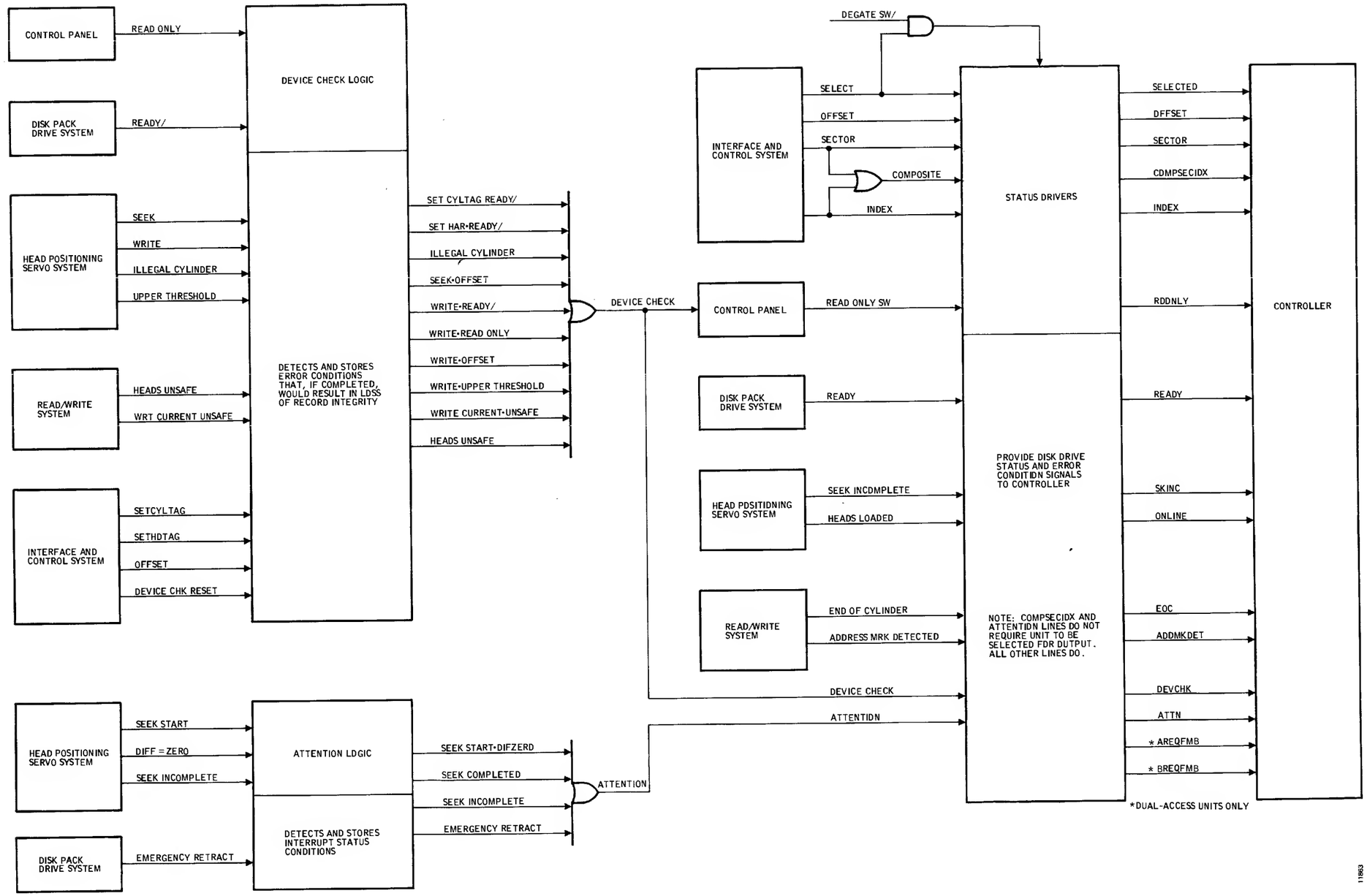

Figure 6-1. Status and Error Detection System, Block Diagram

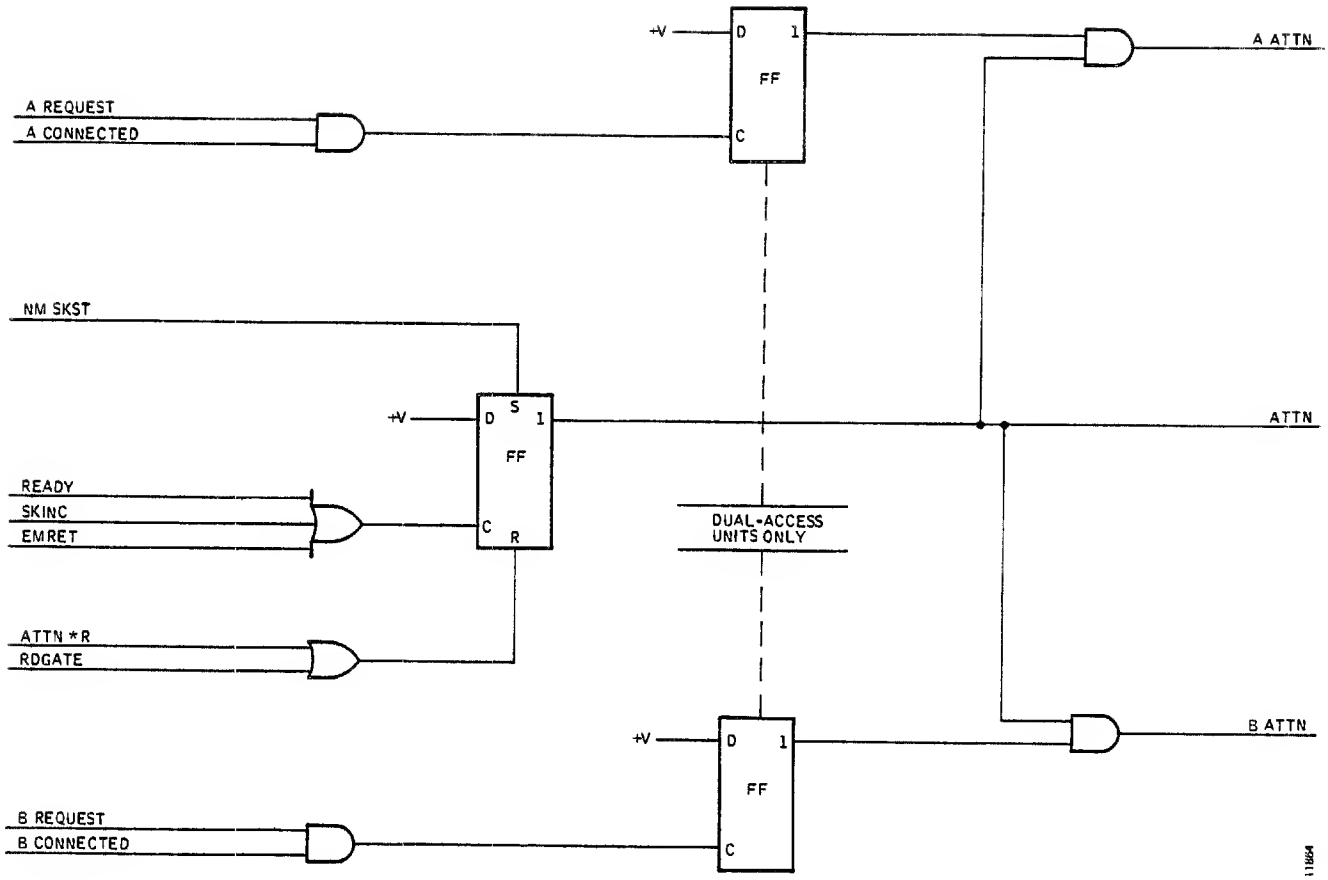

Figure 6-2. Attention Interrupt Logic, Simplified

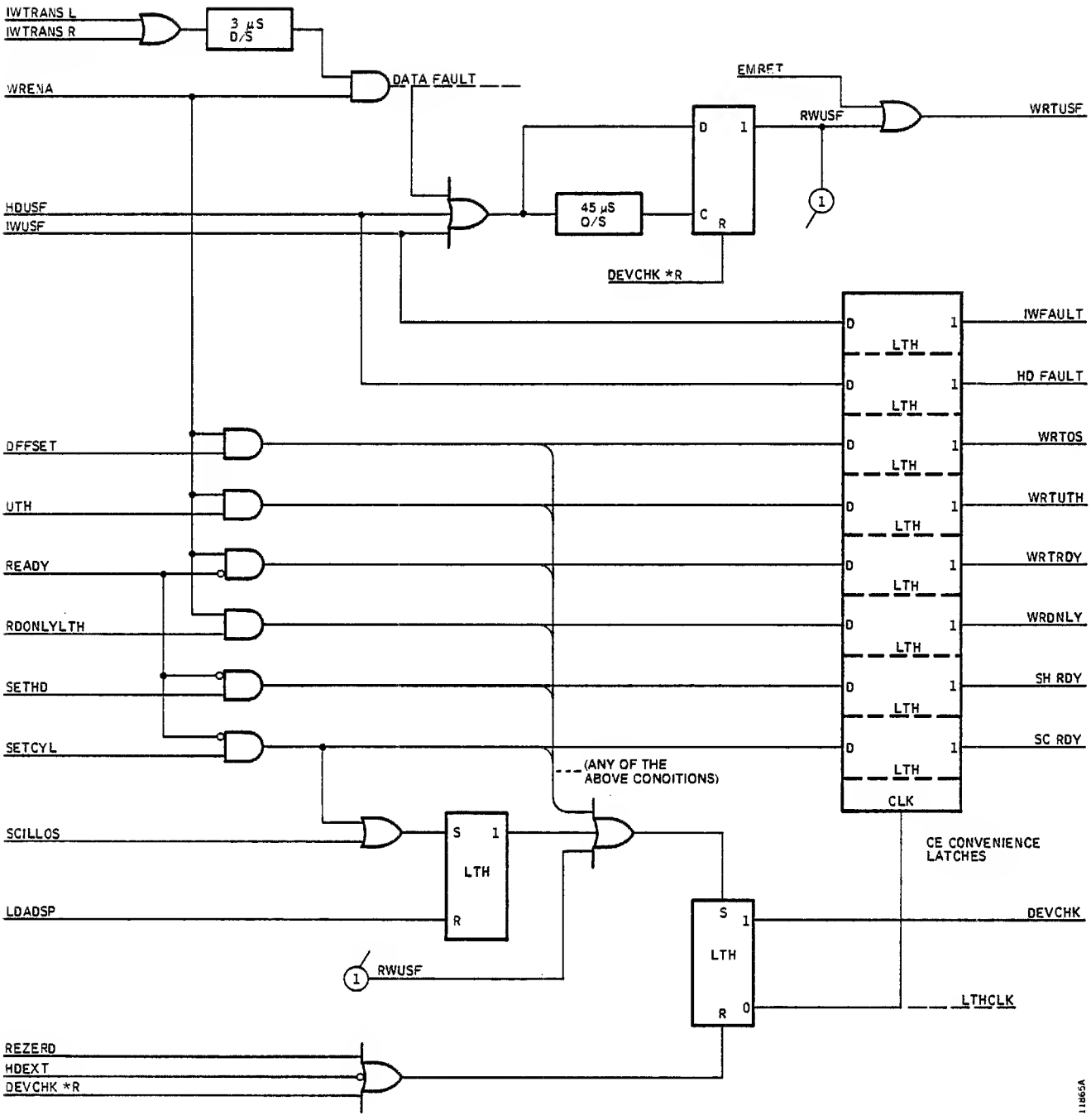

Figure 6-3. Device Check Fault Logic, Simplified

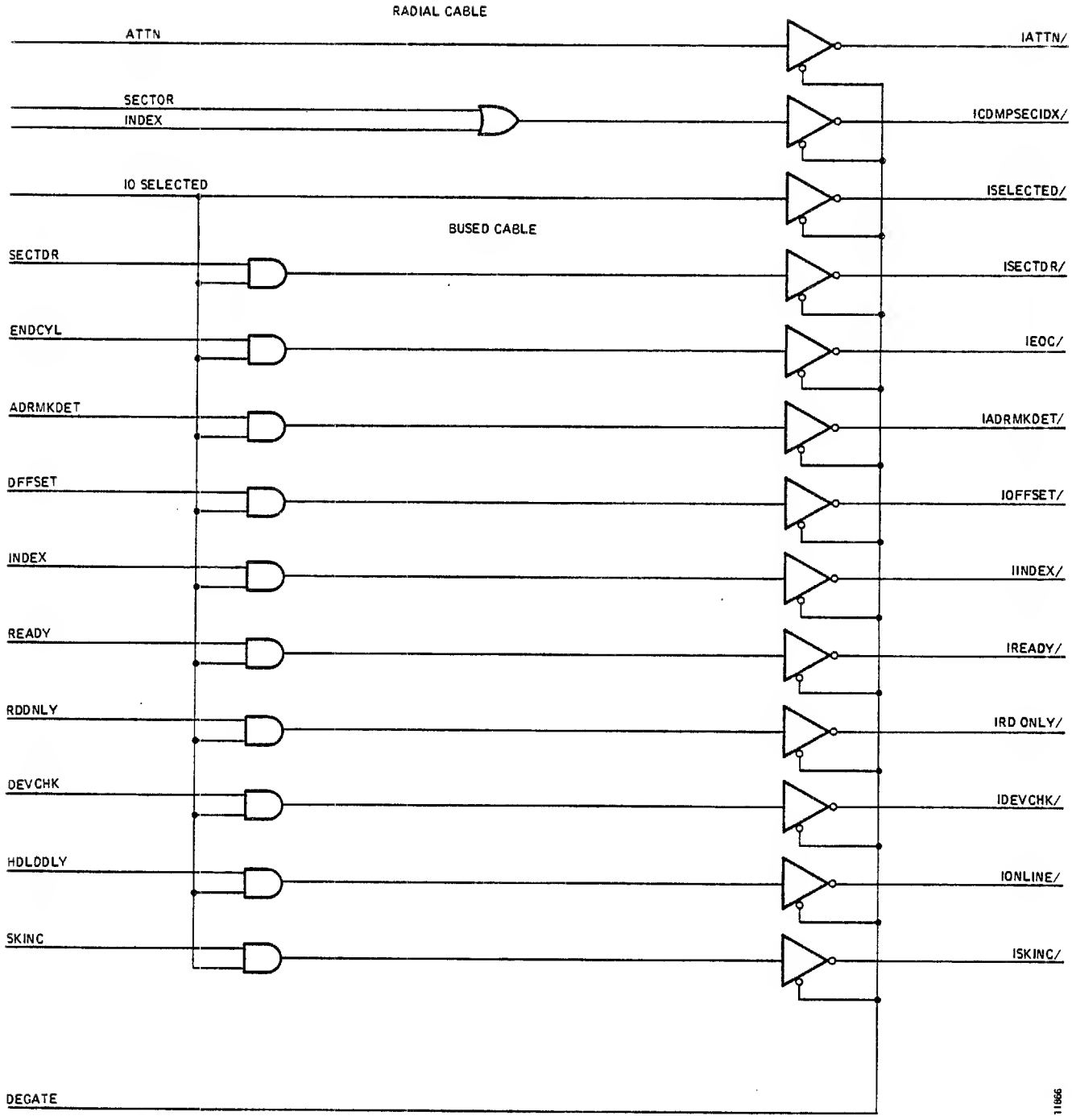

Figure 6-4. Single Access Status Drive Logic, Simplified

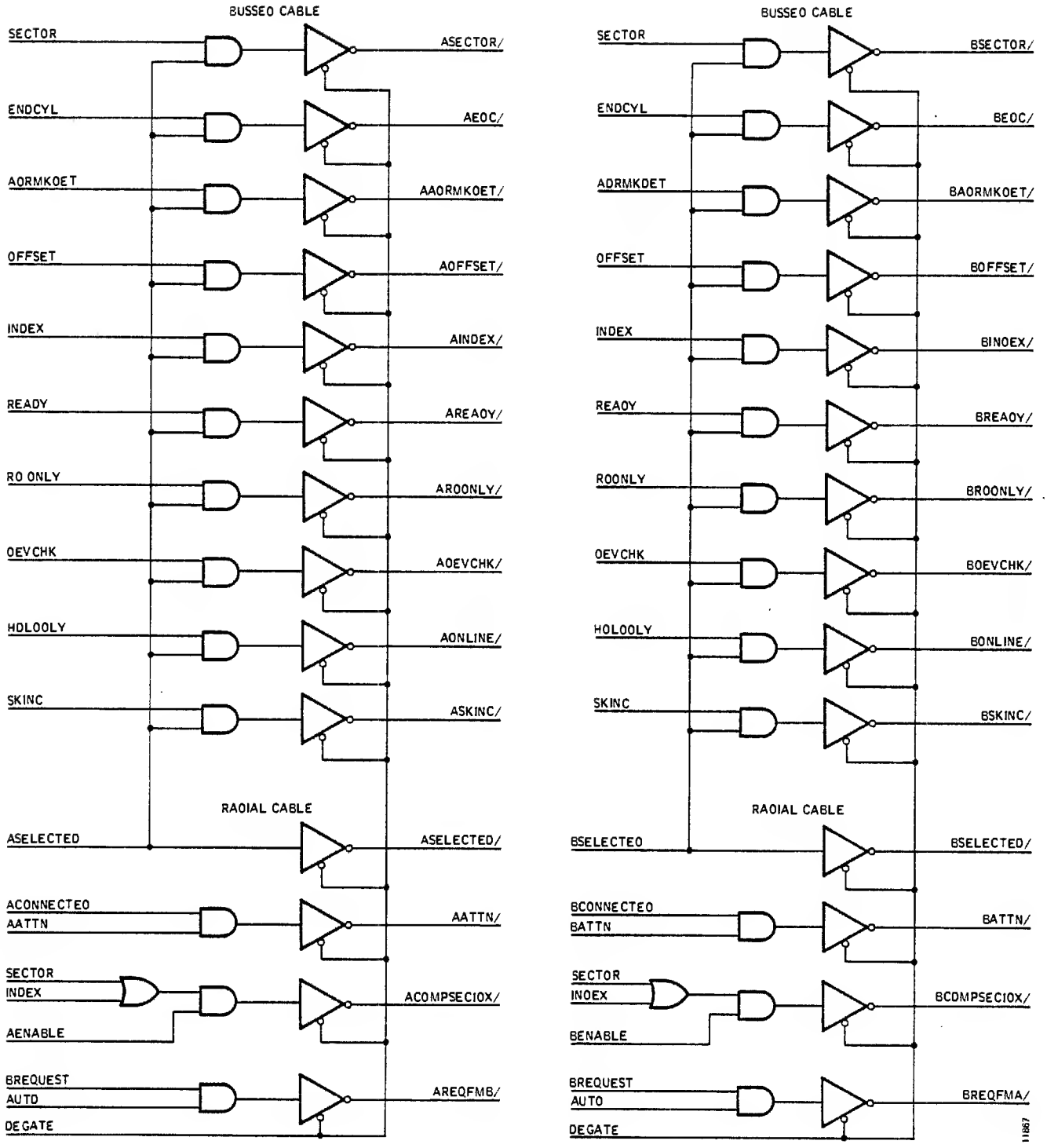

Figure 6-5. Dual Access Status Drive Logic, Simplified

SECTION 7
POWER SUPPLY SYSTEM

The Power Supply System for Trident T200/T300 disk drives is shown in Figure 7-1. These drives accept ac power that is nominally rated at 208/230 volts. However, the drive will operate on voltages from 178 volts to 264 volts; voltages greater than 220 volts require a single-pin wiring change at the input to the power supply.

Ac power from the facility source is applied to the Ac Distribution Box. This assembly contains the line filters, main circuit breaker, Dc Ground switch, and the solid-state switch that controls power to the spindle drive motor. See Figure 7-2. Circuit Breaker CB1 controls power to the power supply, cabinet cooling fans, and the blower motor that supplies air pressurization to the disk pack area. The breaker also supplies power to Solid-State Switch K1, whose operation is controlled by the low-active Drive Motor On (DRMOTON/) signal from the power-sequencing logic. Switch K1 is the control element for the spindle drive motor.

Returning to Figure 7-1, note that the power supply provides both dc and ac outputs. The dc outputs are

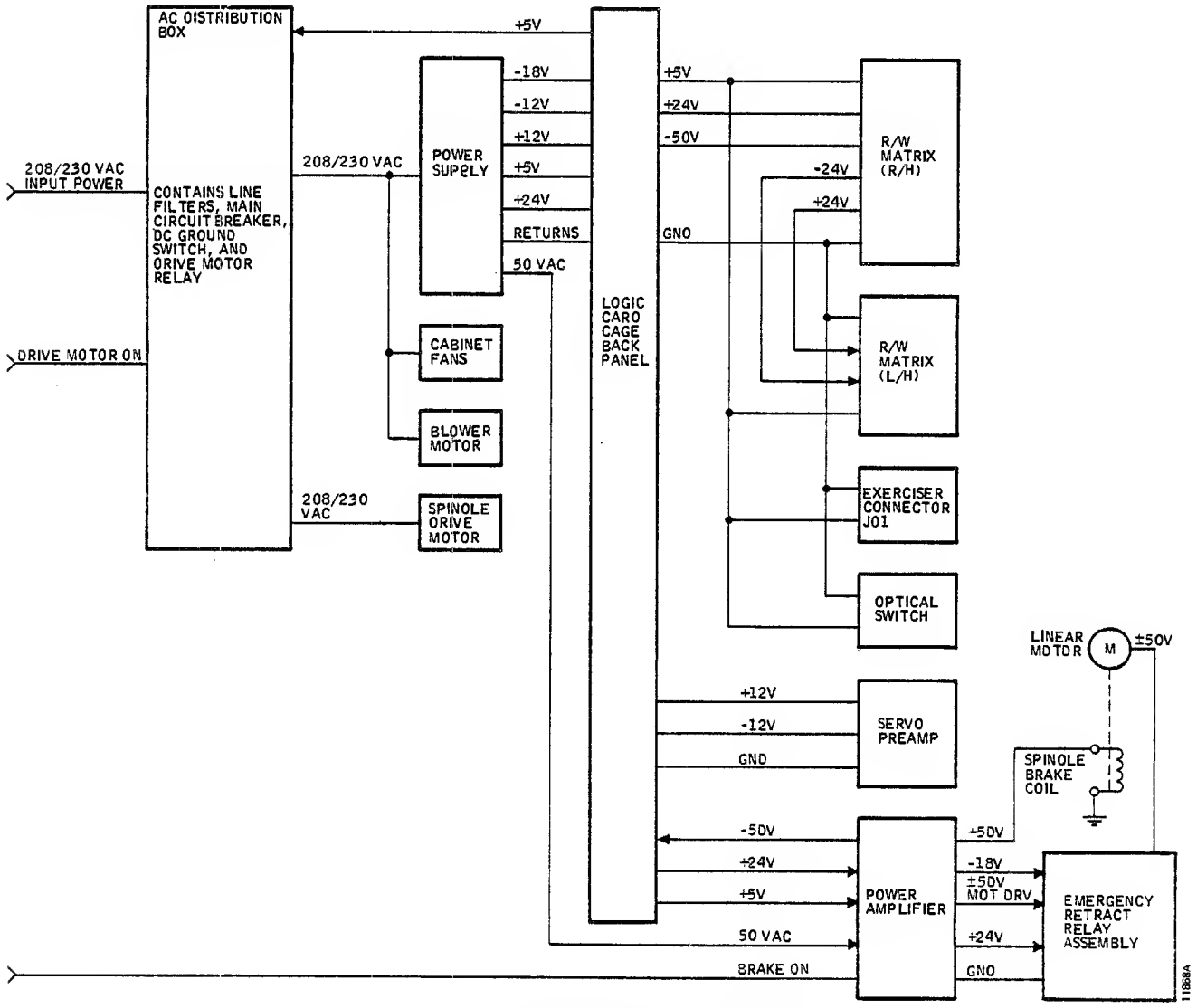

Figure 7-1. Power System, Block Diagram

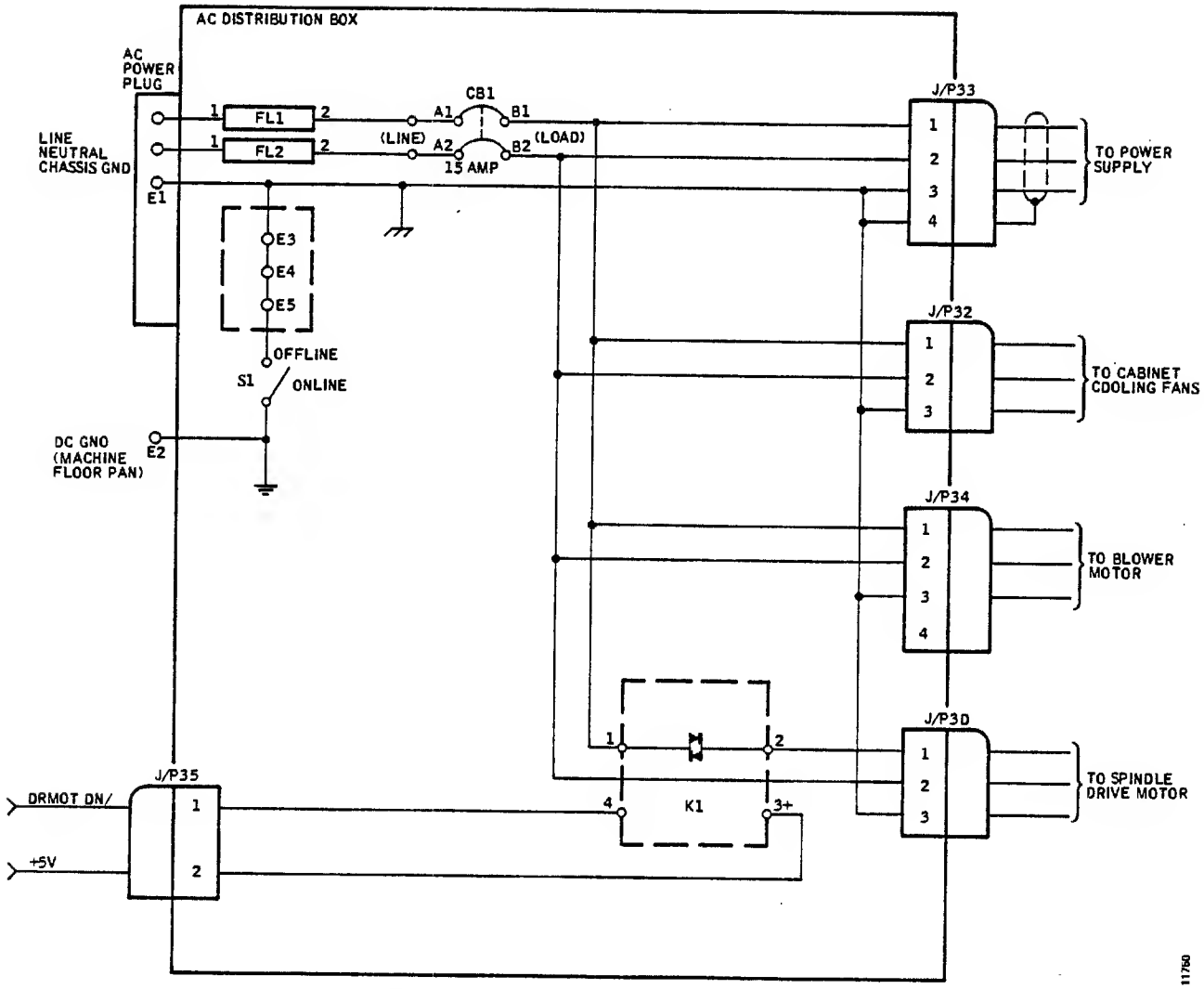

Figure 7-2. Ac Distribution Box Circuits

the operating voltages for the circuit cards and other elements in the drive with the exception of the drive power to the linear motor and the write current. The 50-volt ac output is directed to the Power Amplifier.

A bridge rectifier in the Power Amplifier rectifies the 50 vac into 50-volt dc power. This is the origin of the ±50-volt motor drive power that operates the linear motor. The same 50-volt power is also supplied to the R/W Matrix (R/H), where it is converted to the −24-volt reference source for the write current. The Power Amplifier also supplies +50-volt power to the Spindle Brake Coil when the drive logic generates the BRAKE ON command during power-up and power-down sequences.

A −18-volt raw unregulated output is also generated by the Power Amplifier. This voltage provides power to the Linear Motor during an emergency retract operation. The +24-volt operating power for the Emergency Retract Relay also passes through the Power Amplifier, as does the EMERETRLY signal (not shown) that energizes the relay.

The Logic Card Cage Back Panel serves as the distribution system for dc voltages used throughout the drive as shown on Figure 7-1. Notice also that the −50-volt output from the Power Amplifier to the R/W Matrix (R/H) is routed via the back panel.

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